Substrate Temporary Bonding Supporting Post-Processing Applications

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Temporal Bonding
Thin Substrate Market Drivers

• Electronics trending thinner
• Smart phones, tablets, etc.
• Diced chips are stacked
• Stacked chips used in all functional devices
• Extremely fragile
• Requires a temporary support
Bow/Warp Introduction

Bowing – observed internal stress, metal layers

Full thickness ~ 700um  Thinned ~ 100um

Wafer Bow
Temporary Bonding

- Tunable Force Adhesive
- Thin Solid Material w/ Tensile (T)
- Removal Force R
- Force Angle θ
- Carrier Substrate
- Adhesive Force A
Temporary Bonding

Glass & Ceramic Pieces

Wafers

Panels & displays

Components

Films & coatings

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Adhesive Types & Properties
Silicone Thermoset (catalytic)

Resin monomer (MW & shape) $\rightarrow$ Free-Radical

Activator monomer (MW & shape) $\rightarrow$ Silicone Polymer
Acrylic Thermoset (Free-radical)

Vinyl Group

Acrylate Monomer

R = H, NH2, CH3, C2H5, etc.

Polyacrylate
Adhesive in Several Forms

- Liquid
- Gel
- Film
Tape Designs

- Film
  - Release Layer (PET, Silicone)
  - 1-5 mil
  - Silicone Adhesive
  - Release Layer (PET)
  - Transfer Tape

- Adhesive
  - 1-5 mil
  - Adhesive on backing

- Film + Fiber
  - Release Layer (PET, Silicone)
  - 4-20 mil
  - Fiber (Support)
  - Composite Adhesive
Peripheral Bond

- The adhesive may be applied on the edges of the carrier – known as *peripheral bond*
- Thin substrate is bonded onto carrier
- Adhesive undergoes heat cure
Peel Testing

- 90° Peel test following ASTM protocol
  - 5 mm/s peel speed
  - 1 cm cut width
  - Use of Mark 10 motorized force test stand and M5-10 force gauge with MESUR™ gauge software.
Peel Graph of PCA120612-001
Effects of Post-Bake on Outgassing from Vinyl Silicone

Testing in Air

Temperature (°C)

Thermal Stability %

No PB

PB 250C

PB 300C

PB 350C

Testing in Air

Temperature (°C)

Thermal Stability %

No PB

PB 250C

PB 300C

PB 350C

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Adhesion vs. Formulation

• Adhesion force is tuned by formulation

Peel Force of Aluminum Foil
Adhesive Thickness (4 microns)
Adhesion vs. Cure Mechanism

- Reaction speed plays a role in adhesion
Adhesion vs. Thickness

- Adhesion increases with thickness
Adhesion vs. Bonding Pressure

- Adhesion force increases with pressure
Adhesion vs. Process Temp

- Adhesion force increases with temperature
Adhesion vs. Substrate

- Adhesion force dependent upon substrate

![Graph showing peel force of solid film materials]
### Adhesive Qualities by Application

<table>
<thead>
<tr>
<th>Application</th>
<th>Modulus</th>
<th>Adhesion</th>
<th>Thermal</th>
<th>Uniformity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mechanical (e.g. thinning)</td>
<td>↑</td>
<td>↑</td>
<td>↔</td>
<td>↑</td>
</tr>
<tr>
<td>Vacuum (i.e. PVD, plasma etch)</td>
<td>↔ ↔</td>
<td>↔ ↔</td>
<td>Tool dependent</td>
<td>↔ ↔</td>
</tr>
<tr>
<td>Dielectric cure and/or material anneal</td>
<td>↔ ↔</td>
<td>↔ ↔</td>
<td>↑</td>
<td>↔ ↔</td>
</tr>
</tbody>
</table>

**Full process:**

<table>
<thead>
<tr>
<th>Application</th>
<th>Modulus</th>
<th>Adhesion</th>
<th>Thermal</th>
<th>Uniformity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thinning + backside Process + PI curing</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
</tr>
<tr>
<td>Flexible display (poly-Si anneal)</td>
<td>↔ ↔</td>
<td>↔ ↔</td>
<td>↑</td>
<td>↑</td>
</tr>
<tr>
<td>Pkg EMI Shielding (low temp PVD)</td>
<td>↔ ↔</td>
<td>↔ ↔</td>
<td>↔ ↔</td>
<td>↔ ↔</td>
</tr>
</tbody>
</table>
Substrate Characterization
Wafers

- Wafers thinned to <100um
- Carriers are required
- Debonding generates problems, can be a bottleneck, high cost, and source of yield loss
Carriers

- Silicon
- Glass
- Sapphire
- Tape

Porous Carriers
Perforated Glass, 50 μm

Surface Scan shows the divots from glass pores

Black: Surface Scan of Perforated carrier
Red: Surface Scan of ground wafer with perforated carrier
Porous Carrier

**Benefits**
- Thermal & chemical resistant
- Simple bond, high adhesion
- Accepts many adhesive types
- Passive debond (chemical diffusion)
- Device wafer on film frame
- Recycle >10X

Device Wafer
- Adhesive over Planarization Coat

Carrier
- Porous Layer w/ Edge Exclusion
Porous Metal Carrier

Polishing to TTV
Surface Treatment

Without Exclusion Layer

With Exclusion Layer

Wetting

No wetting
Bonding & Debonding
Peel De-bond Mechanics

Common peel separation

Thermal-slide (shear)
Peel Configurations

- Line peel separates from adhesive in specific zone
- Adhesion force is lower, shear, and stress

Line Vs. Surface Area Configuration

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Deflection at Distance from Fixed End

Force is Fixed
Equivalent Deflection at Different Distances

Distance from Fixed End (m)

Multiplication of Force
Relative Peel Force

Lowest  Med-Low  Medium  High

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Controlled Adhesion: Roll Peel

Must Be Custom Equipment
Roll-Tool Mechanics
Performance
Roll-Tool Repeatability

Peel Force of PCA130930-001 after 350°C(15min)

Repeatable Roll-Tool Peel Forces

Target <12 N/cm

1st 350°C Cycle: 5.395
2nd 350°C Cycle: 5.6375
3rd 350°C Cycle: 5.395
4th 350°C Cycle: 5.395

* Cure Program: 150C(10min), 350C (15min) based on TGA Results
Engineering Polymers

PBI Tg = 427 °C

PI Tg = 370 °C
Typical PI Transparency Thermal Trend

![Graph showing the typical PI transparency thermal trend with wavelengths ranging from 300 to 800 nm. The graph depicts the percentage transmission (%T) for temperatures of 350°C, 400°C, and 450°C under an inert N2 atmosphere.]
Case Histories
Ex. 1 – Die bond on TSI BGA

- Thin Silicon Interposer (TSI)
- Substrate ~100um thickness
- Underlying bumps ~100um height

Top side
Bottom side
(contains solder bumps)
Adhesive Application and Bonding

1 Substrate w/Topography

2 Application Coverage

3 Cure to Planarize

4 Apply/Cure to Carrier

5 Apply to Substrate Bond to Carrier

6 Cure to Mount

Recyclable porous substrate
Post-Bonding Process

7 Customer Process
Bonded interposer
attach chips to interposer
Reflow 250-300C

8 Debond & Cleans
Debond and Cleans
rinse, dry
Recycle carrier

9 Acquire Final Product

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Adhesive Planarization

No adhesive

Adhesive

~75% Bump height
Planarization and Thermal

- Voids -

No Voids

Serious Damage

No Damage

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Porous Carrier

Porosity higher for inside material (A). Outer coating (B) is lower porosity

A = 0.5 – 0.8mm
B = 0.1 - 0.25mm
C = 0.5 – 1mm

TSI on adhesive
Results – baseline TSI
Results – Bonded TSI

Variation <12um
Profilometry Measurement of Bow vs. Process Condition

- Max
- Ave

Measured Bow (µm)

<table>
<thead>
<tr>
<th>Process Condition</th>
<th>Free Standing Interposers</th>
<th>Affixed Interposers</th>
</tr>
</thead>
<tbody>
<tr>
<td>H1, H2, L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1, 2, F</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NW1, NW2, NW3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Type
- 1, 2, F Peripheral
- NW Porous Subst

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Bow Reduction of Affixed Interposer Die

Reduction as % of original condition

<table>
<thead>
<tr>
<th>H1</th>
<th>H2</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>69.9%</td>
<td>87.8%</td>
<td>73.8%</td>
</tr>
</tbody>
</table>

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Ex. 2 – Wafer support (solar)

1. Implant (Donor Substrate)
2. Exfoliation – 4um thick
3. High temperature anneal
4. Temporary carrier bond
5. PVD metal (60C, vacuum)
6. Permanent substrate bond
7. Debon德 temporary carrier
7. Finish processing
Temporary Bond – Solar

- 4um thin wafer
- Urethane thermoplastic
- Liquid adhesive – proof of concept, complete process development, tooling
- Film adhesive, converted/stamped, roll-to-roll operation on a panel operation
Liquid Conversion to Film

**Liquid Spin-Coat**
- Thin wafer & Carriers
- Spin Coating
- Cure & Bonding
- Cell Build
- Single-Wafer De-bonding
- Dirty wafer & Carriers
- Clean wafer & Carriers

**Film Lamination**
- Thin wafer & Carriers
- Cure & Bonding
- Cell Build
- Single-Wafer De-bonding
- Dirty wafer & Carriers
- Clean wafer & Carriers
Ex. 3 – Curved Display

- Cast liquid PI substrate
- Adhesive cured on glass carrier
- Lift-off/peel force tuned for HVM needs
PI or Similar Coating

Daetec’s Polyimide

**Slit Coating:**
1. Adjust Gap height (10-40µm)
2. Apply

**Spin Coating:**
1. Dispense
2. 1000-2000rpm (60sec)

**Curing**
1. 150°C (5min)
2. 250°C (15min)
3. 350°C (10min)

Cured DaeCoat™ 310
Adhesive Force of DaeCoat™ 315 With Daetec’s PI

Peel Force (gF/cm)

- 9:1 A:B
- 8:2 A:B
- 7:3 A:B
- 6:4 A:B
- 5:5 A:B

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Typical Thin Substrate Support

- Tape
- Vacuum Chuck
- Carrier & Adhesive
Ex. 4 – EMI Shielding on Devices

- Cast liquid PI substrate
- Adhesive cured on glass carrier
- Lift-off/peel force tuned for HVM needs

LGA (flat metal pads)

Size 25 X 25mm

BGA (>200um metal balls)

Bottom must be protected
Small Devices for Thermal Processing

**Appearance of Bottom**

<table>
<thead>
<tr>
<th>Name</th>
<th>#1</th>
<th>#2</th>
<th>#3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>0.95cm x 0.95cm</td>
<td>1.65cm x 1.15cm</td>
<td>0.95cm x 0.95cm</td>
</tr>
<tr>
<td>Overview</td>
<td><img src="image1.png" alt="Image of #1" /></td>
<td><img src="image2.png" alt="Image of #2" /></td>
<td><img src="image3.png" alt="Image of #3" /></td>
</tr>
<tr>
<td>Microscopic Picture</td>
<td><img src="microscopic1.png" alt="Microscopic Picture of #1" /></td>
<td><img src="microscopic2.png" alt="Microscopic Picture of #2" /></td>
<td><img src="microscopic3.png" alt="Microscopic Picture of #3" /></td>
</tr>
</tbody>
</table>
BGA Pkg Description

Many packages exist

Bottom (balls) & top

Bottom (balls)
Topography <300um

Top (black epoxy)

Size 25 X 25mm (above)
Can be much smaller

Bottom must be protected
EMI Shielding

Bottom (balls)

Top (black epoxy)

Top (and sides) must be coated with EMI shielding metal

Bottom must be protected from EMI coating
EMI Shielding

Top is an epoxy molding compound

EMI Shielding
Metal coatings
3-6um Cu
~0.2um “sandwich” – top & bottom of Cu (Ti or SUS)
EMI Shielding

- EMI Coating on Epoxy Molding Cmpd
- Ti or SUS (0.2um)
- Cu (3-6um)
- Ti or SUS (0.2um)
- Epoxy Molding Compound
- Corrosion Protection
- EMI
- Adhesion & Barrier
Current Process Flow

Pkgs start & finish in JEDEC trays

Pkg Affixing & Removal

Adhesive Process

EMI Shielding Tool (Vacuum PVD)
Component Bonding

Sealed edge
Surface Scan (Bottom of Substrate #1)

Length of the Scan

Angstrom

Metal

Plastic

Peak to Valley = 55um

Warpage = 35um

Not Significant

microns

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Surface Scan (Top of Substrate #1)

Length of the Scan

Warpage = 35 microns

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Substrate Description

Warpage = substrate variation, edge to center (no topography)
Peak to valley = min to max (with topography)
# Ability to Bond & Seal w/Topography

Use of various DaeCoat products

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Peak to Valley (µm)</th>
<th>Warpage (µm)</th>
<th>Adhesive thickness &lt;60µm</th>
<th>Adhesive thickness &gt;60µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>55</td>
<td>35</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>#2</td>
<td>14</td>
<td>&lt;5</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>#3</td>
<td>26</td>
<td>23</td>
<td>B</td>
<td>B</td>
</tr>
</tbody>
</table>

A= Bond + Edge Seal (Ideal Process)
B= Bond
Summary

• Temporary bonding applied to wafers, displays, and devices – substrate support
• Must characterize substrate
• Choose adhesive and match to process needs
• Results suggest adhesive and carriers are demonstrated for substrates 4-10um, flexible, crystalline, using chemical and mechanical debond
Contact for More Information

• DAETEC provides development, consulting, and technical training/support to solve manufacturing problems and introduce new options of doing business.

• Diversified Applications Engineering Technologies (DAETEC)
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