Substrate Temporary Bonding Supporting Post-Processing Applications

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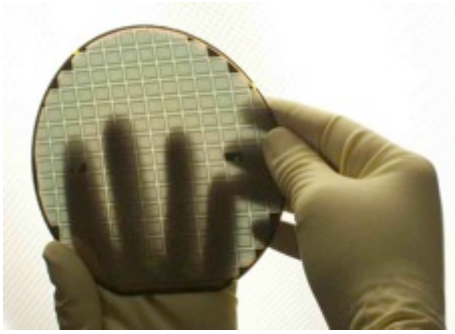
Temporary Bonding

Thin Substrate Market Drivers

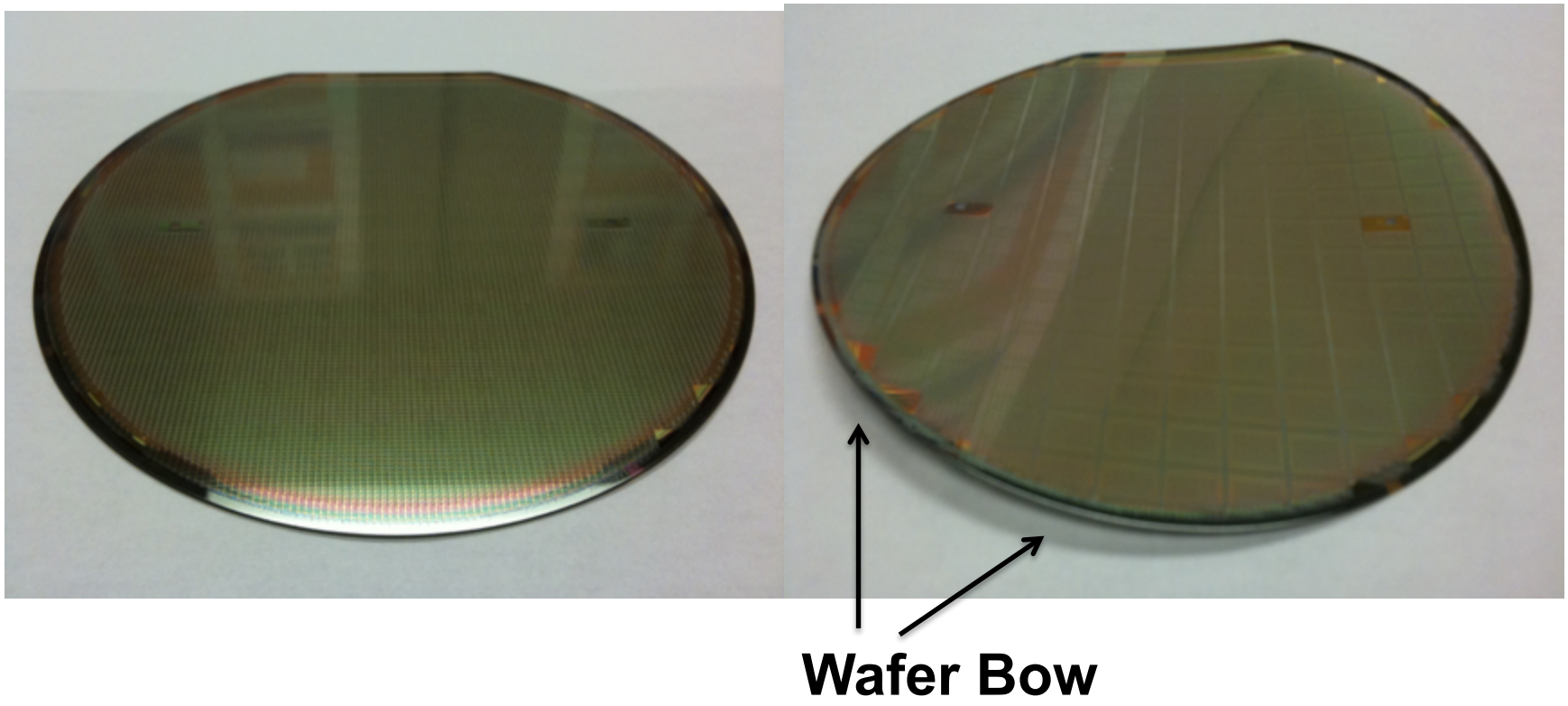
- Electronics trending thinner
- Smart phones, tablets, etc.
- Diced chips are stacked
- Stacked chips used in all functional devices
- Extremely fragile
- Requires a temporary support



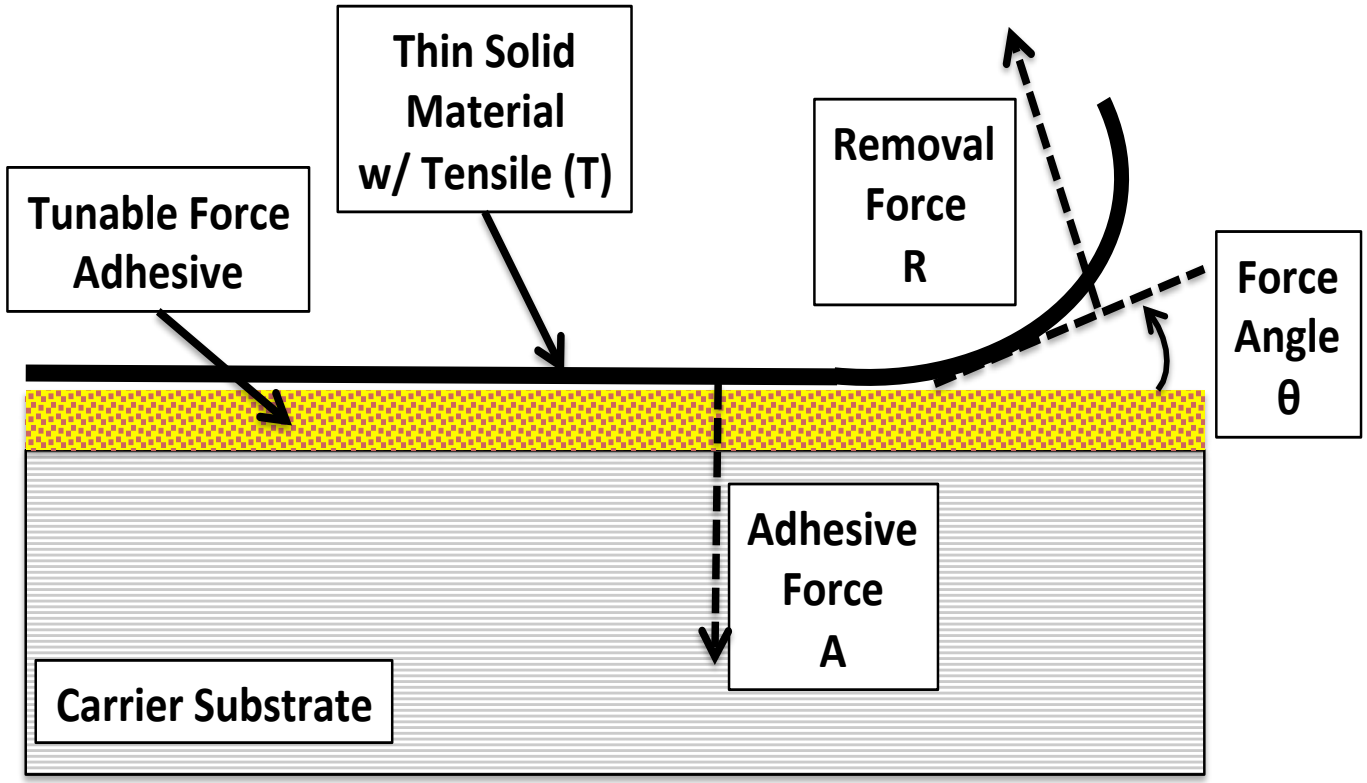
Bow/Warp Introduction

Bowing – observed internal stress, metal layers

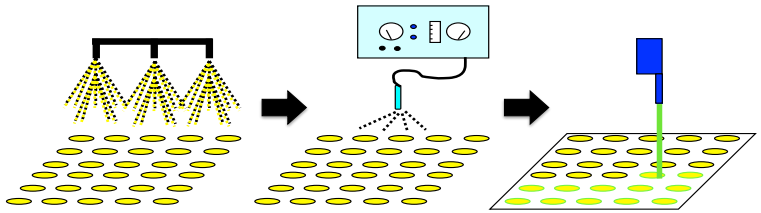
Full thickness ~ 700um **Thinned ~ 100um**



Temporary Bonding

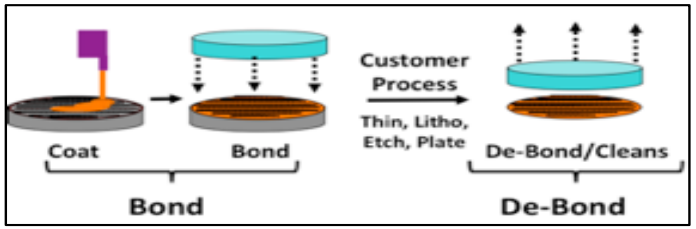


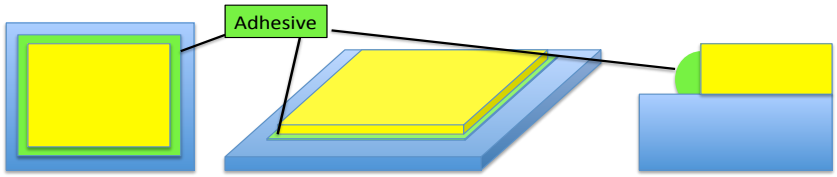
Temporary Bonding



Glass & Ceramic Pieces

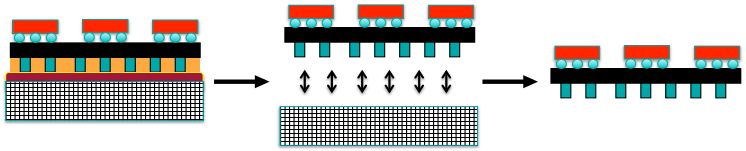
Wafers

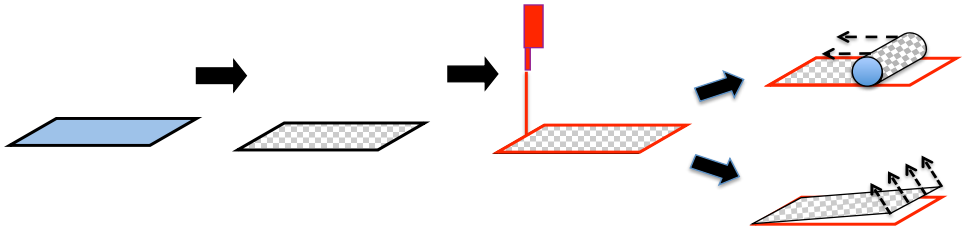




Panels & displays

Components

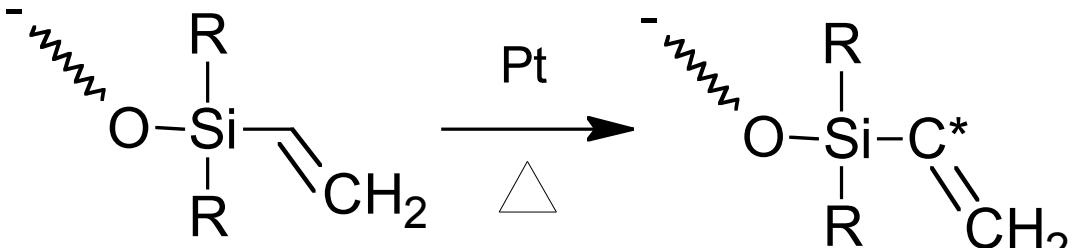




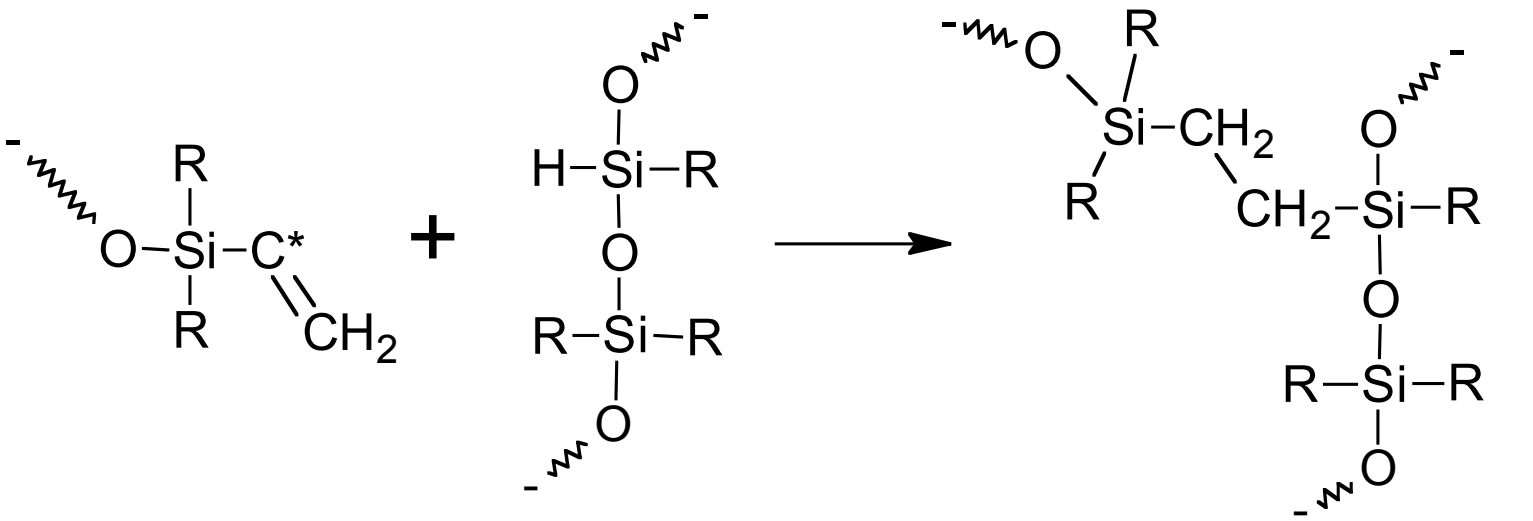
Films & coatings

Adhesive Types & Properties

Silicone Thermoset (catalytic)

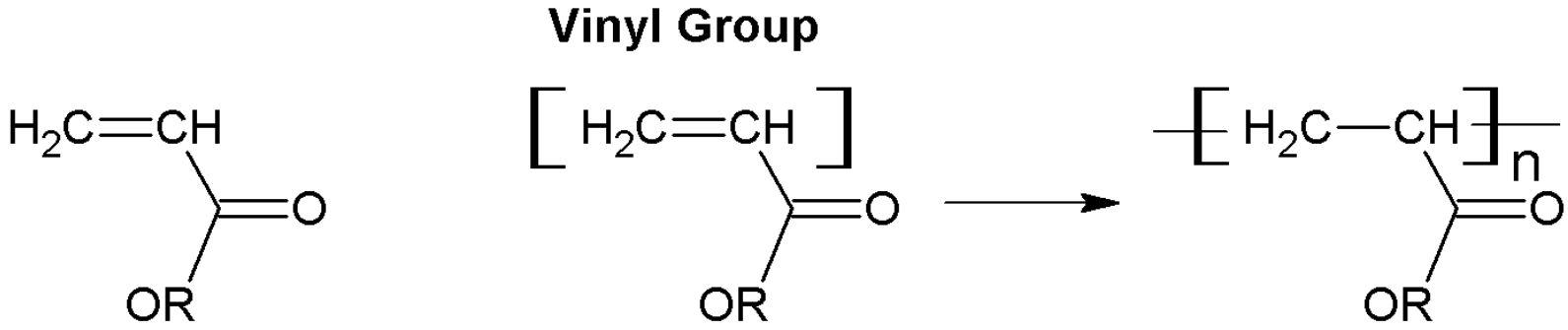


Resin monomer (MW & shape) **Free-Radical**



Activator monomer (MW & shape) **Silicone Polymer**

Acrylic Thermoset (Free-radical)



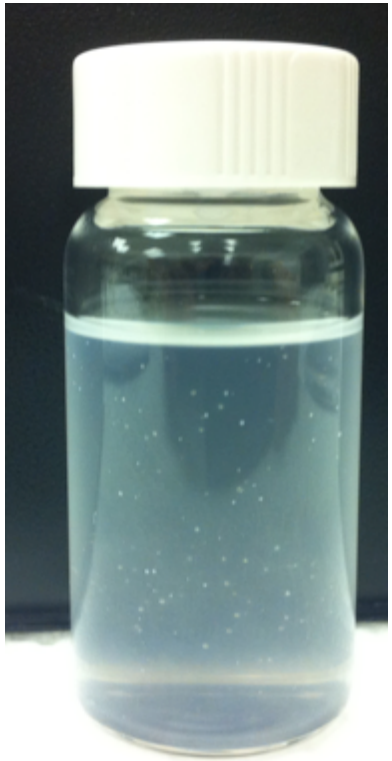
Acrylate Monomer

R = H, NH2, CH3, C2H5, etc.

Polyacrylate

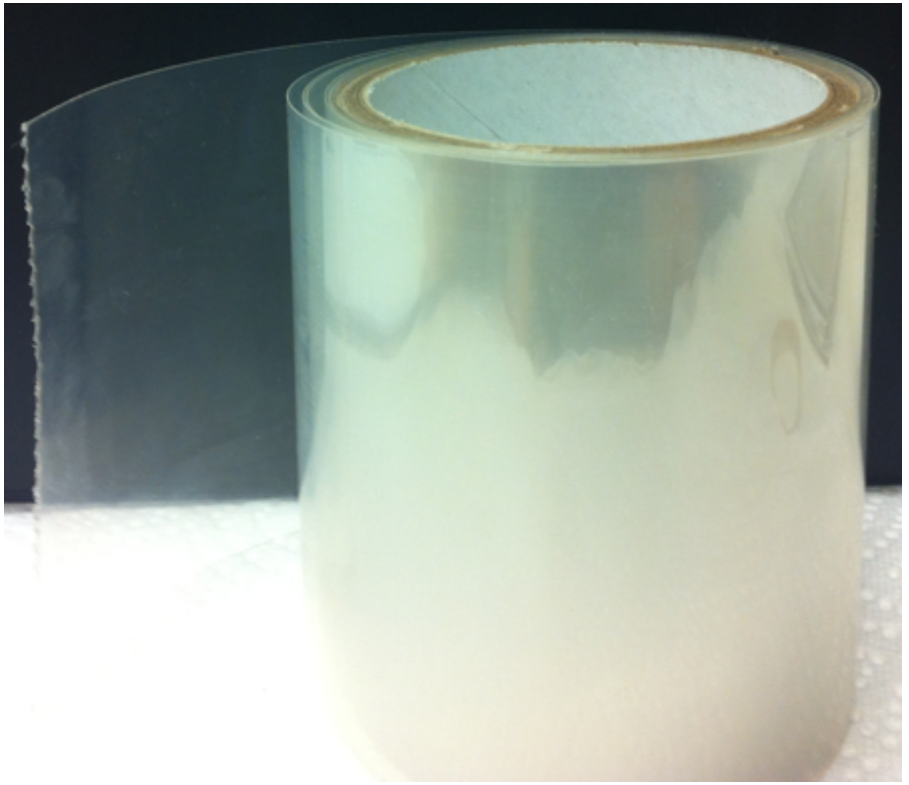
Adhesive in Several Forms

Liquid

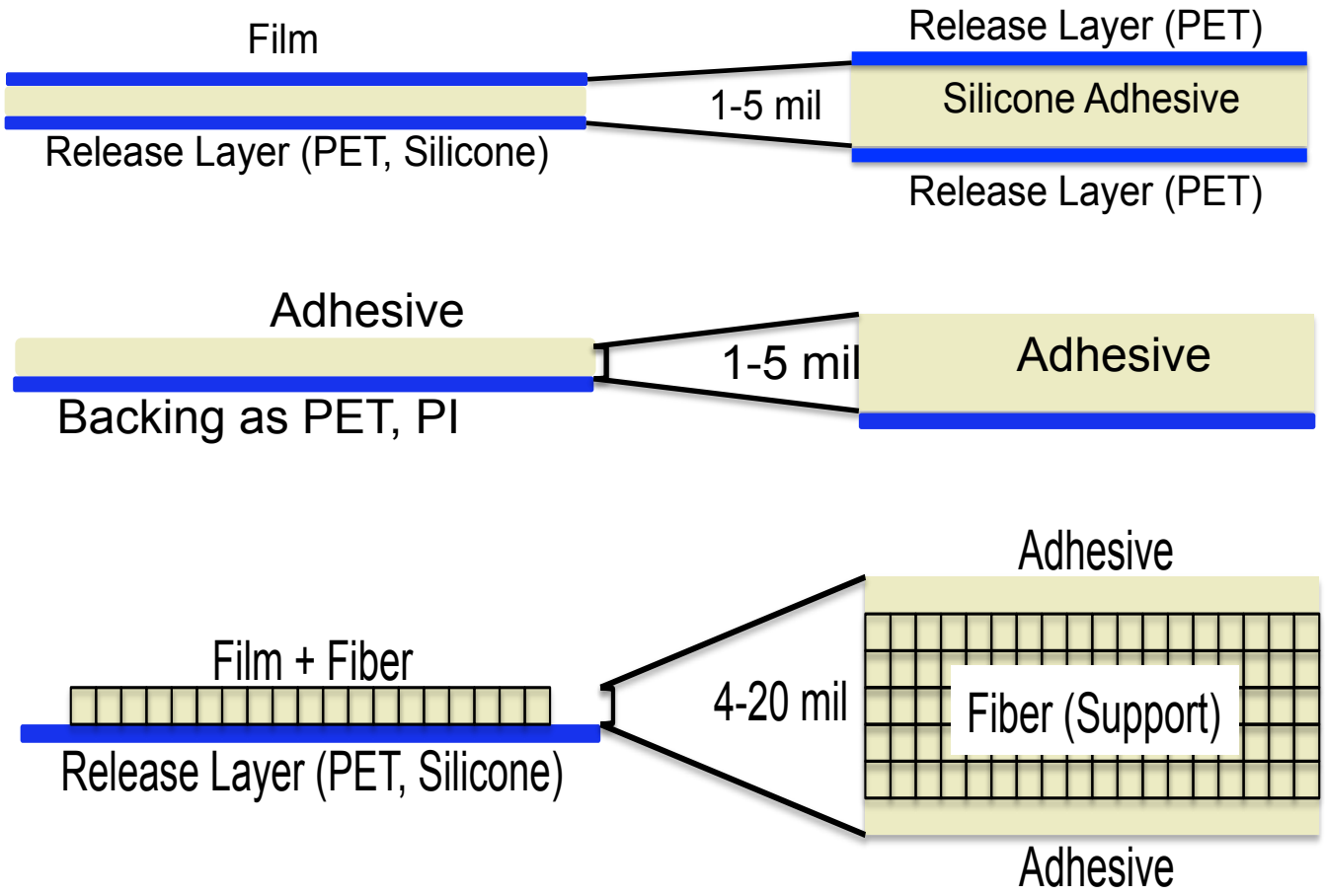


Gel

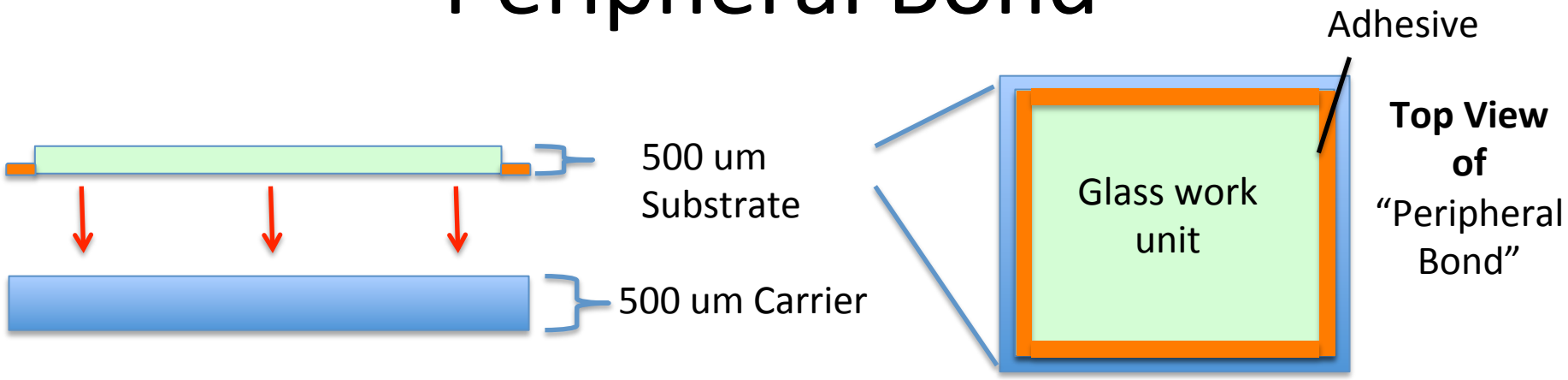
Film



Tape Designs



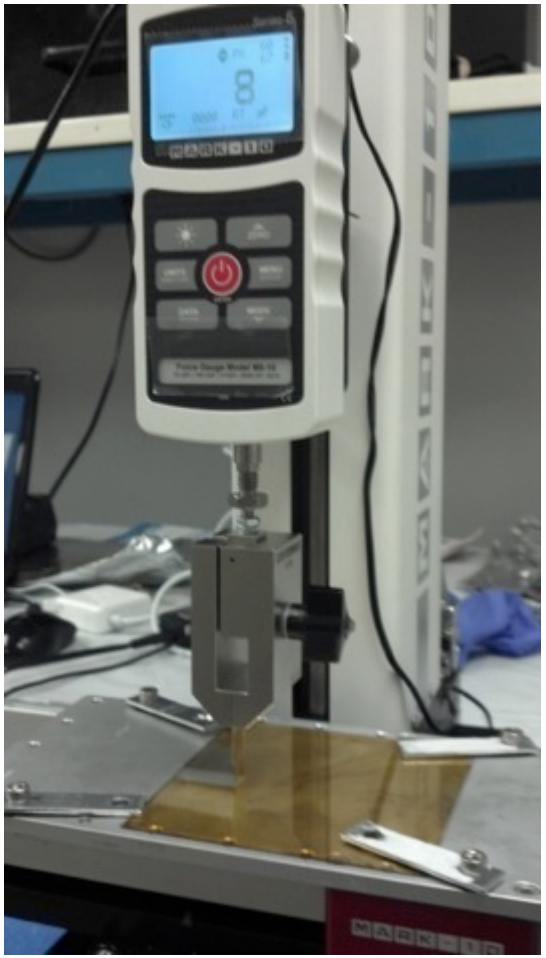
Peripheral Bond

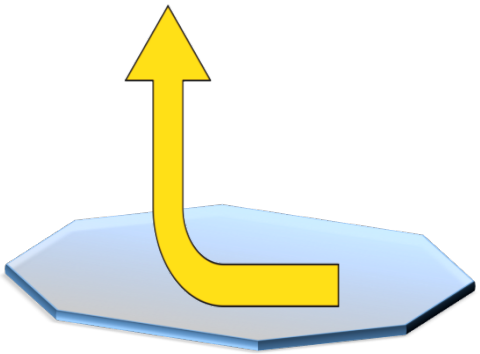


- The adhesive may be applied on the edges of the carrier – known as *peripheral bond*
- Thin substrate is bonded onto carrier
- Adhesive undergoes heat cure

✪ 7.periph. bond

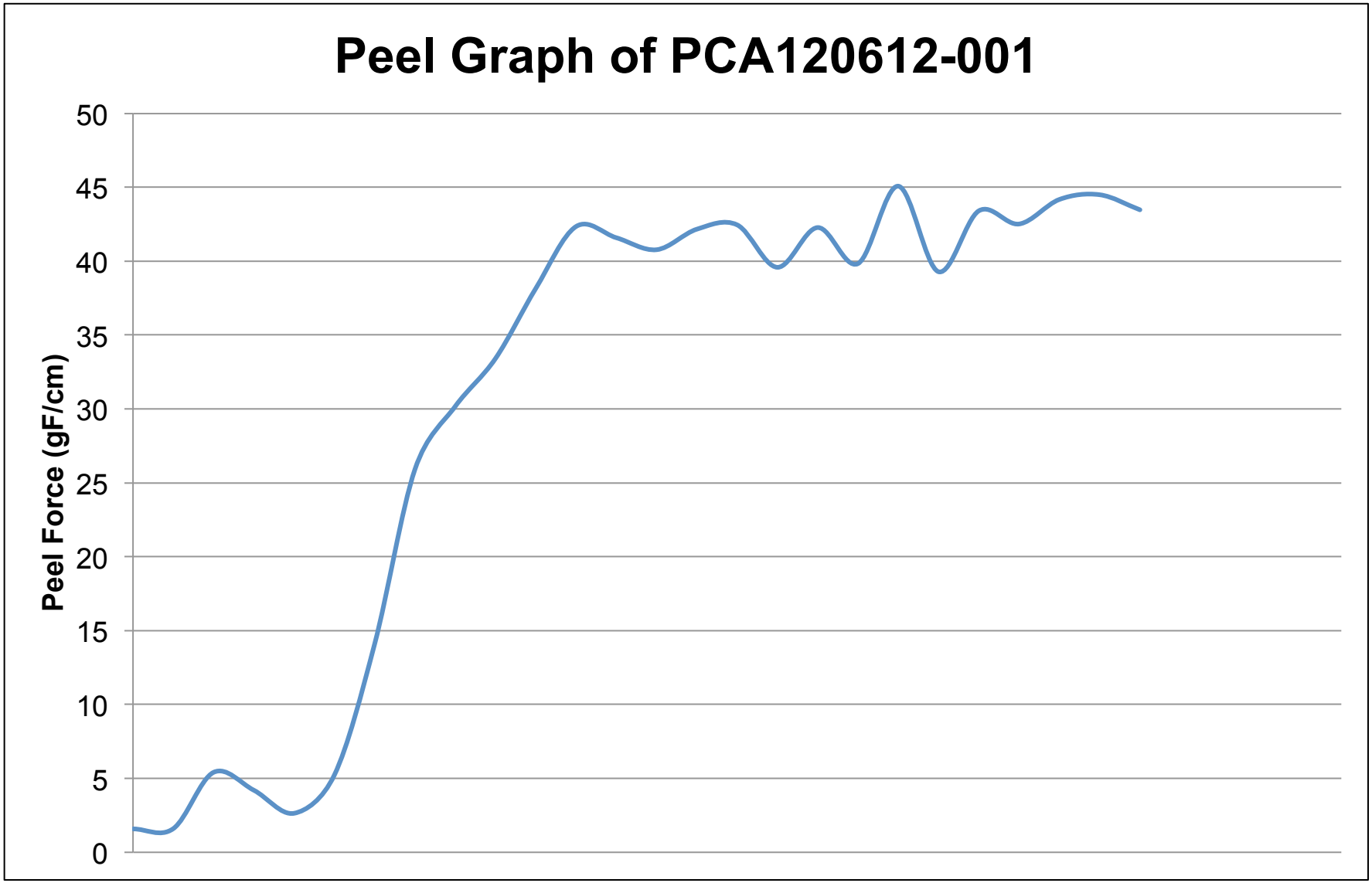
Peel Testing

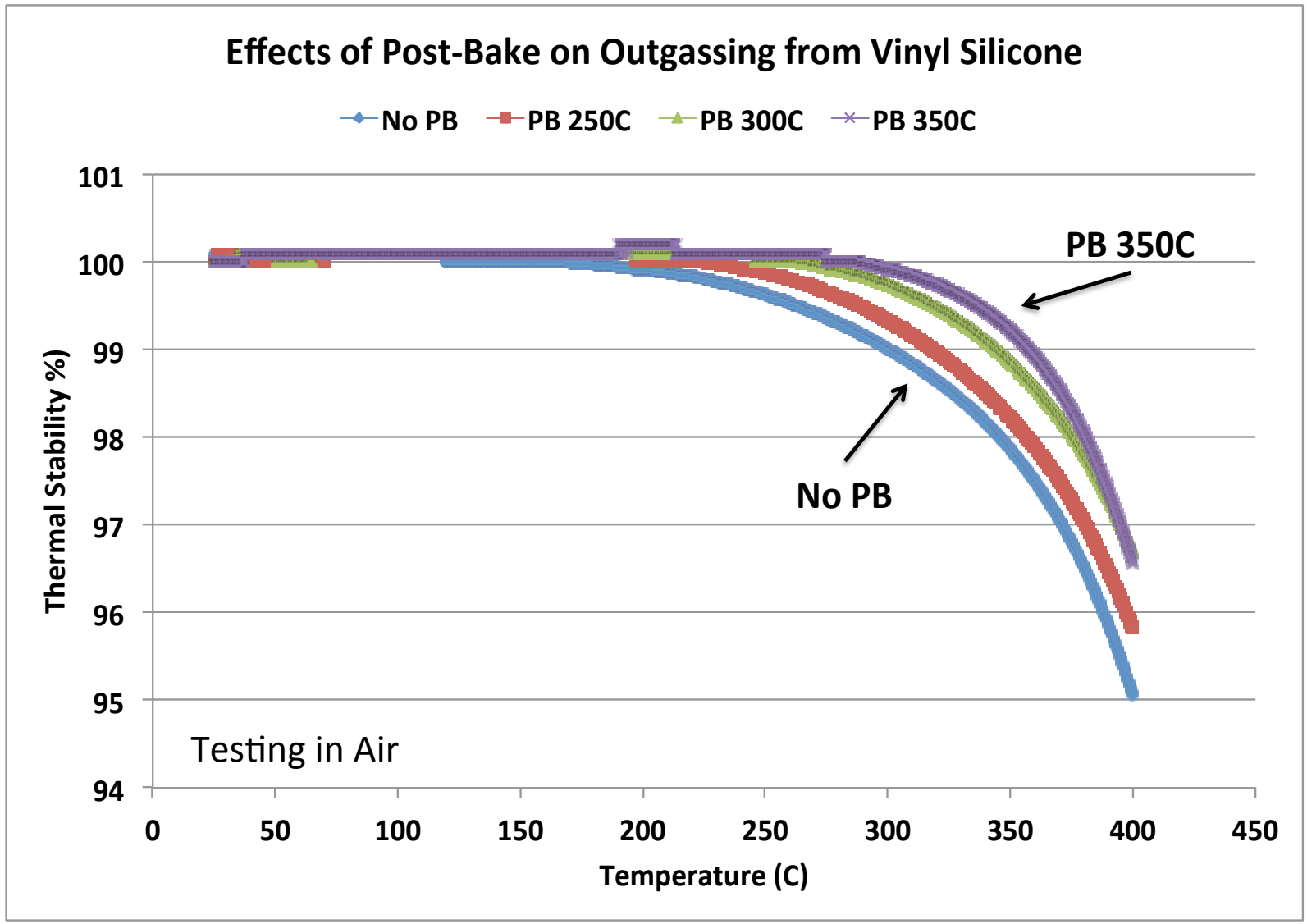




90 degree peel Orientation

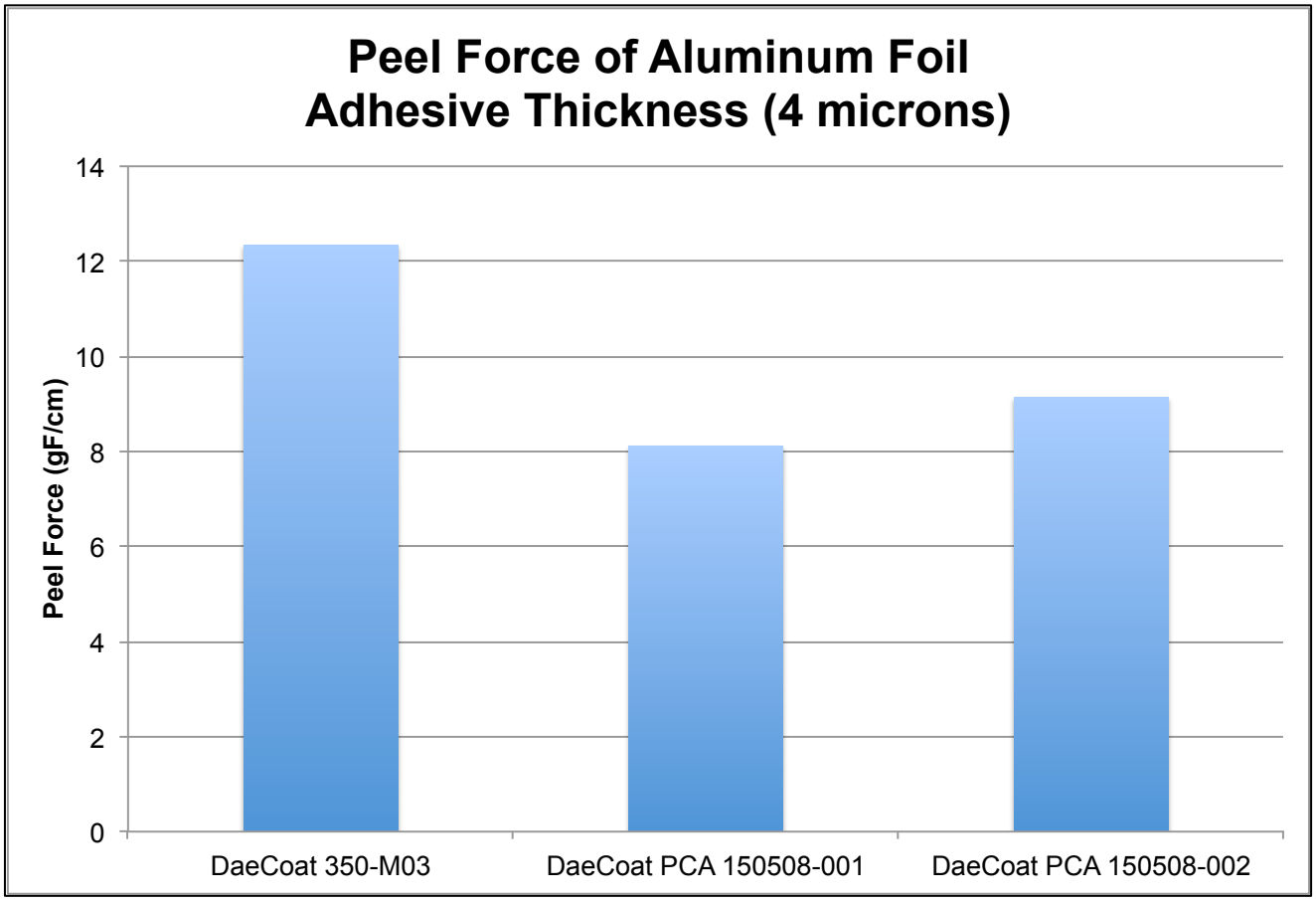
- 90º Peel test following ASTM protocol
- ➢ 5 mm/s peel speed
- ➢ 1 cm cut width
- ➢ Use of Mark 10 motorized force test stand and M5-10 force gauge with MESUR™ gauge software.


Peel Graph of PCA120612-001
Peel Force (gF/cm)
50
45
40
35
30
25
20
15
10
5
0


Effects of Post-Bake on Outgassing from Vinyl Silicone
No PB
PB 250C
PB 300C
PB 350C
Thermal Stability %)
101
100
99
98
97
96
95
94
0
50
100
150
200
250
300
350
400
450
Temperature (C)
PB 350C
No PB
Testing in Air

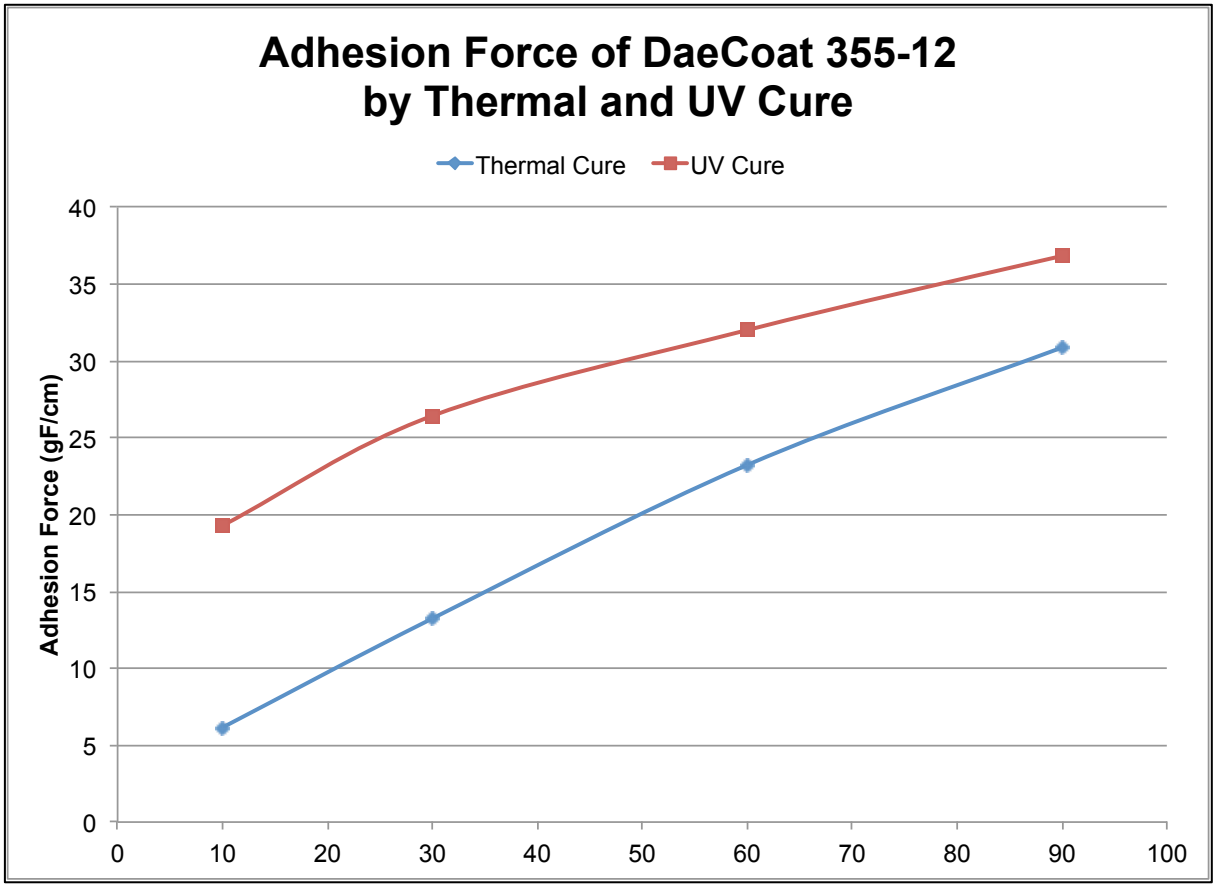
Adhesion vs. Formulation

- Adhesion force is tuned by formulation



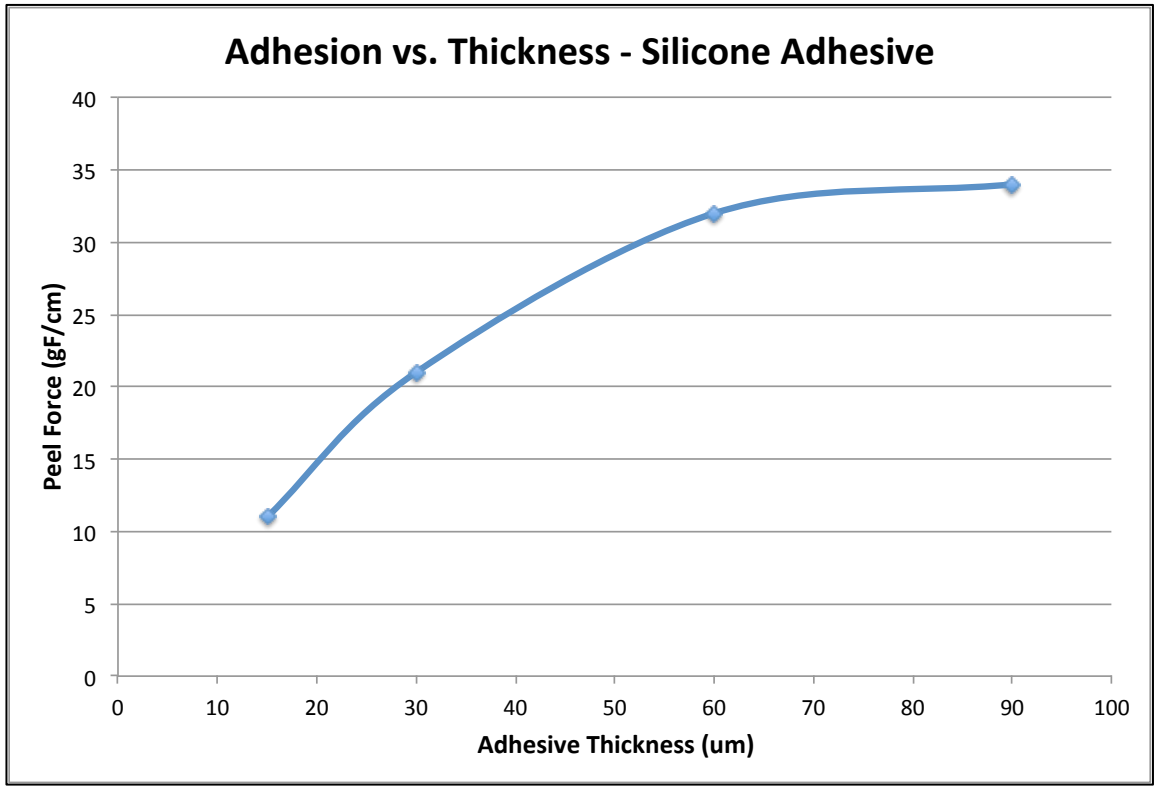
Adhesion vs. Cure Mechanism

- Reaction speed plays a role in adhesion



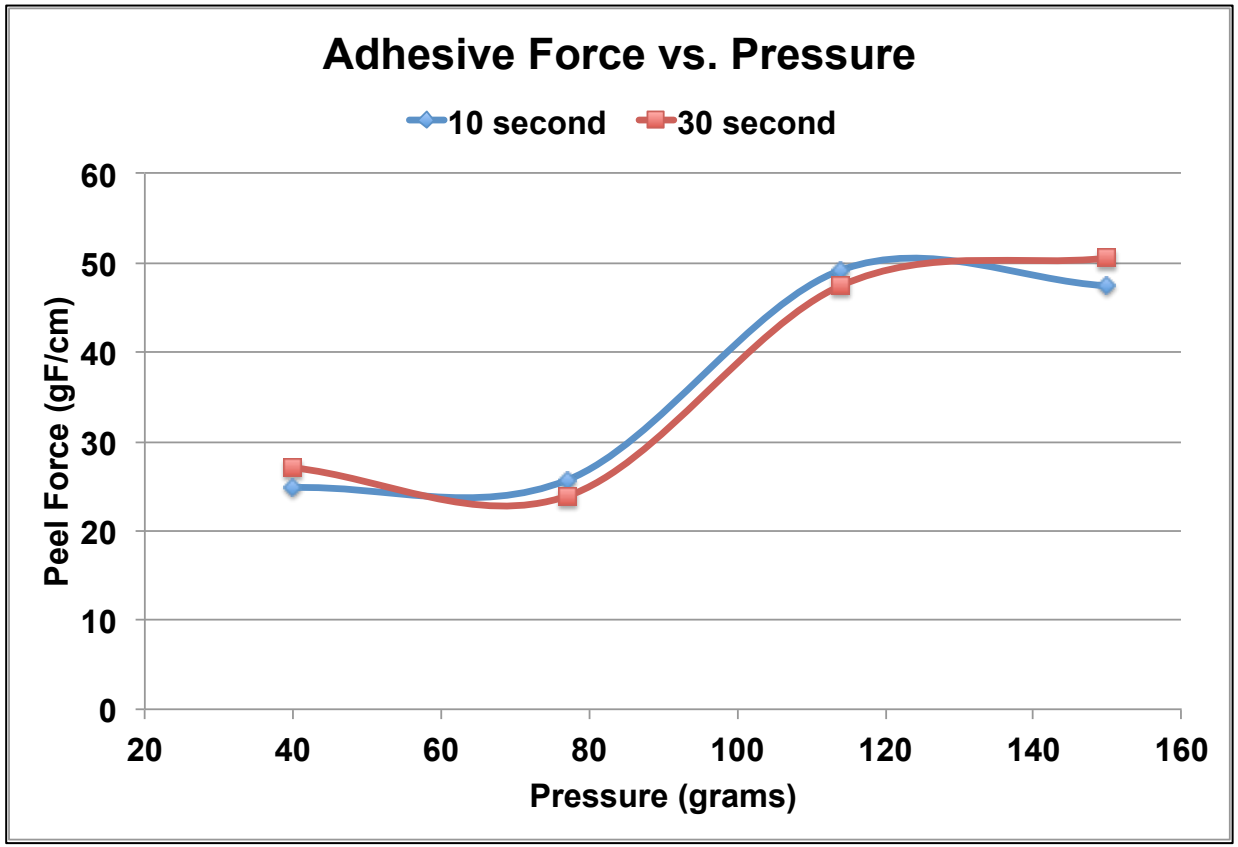
Adhesion vs. Thickness

- Adhesion increases with thickness



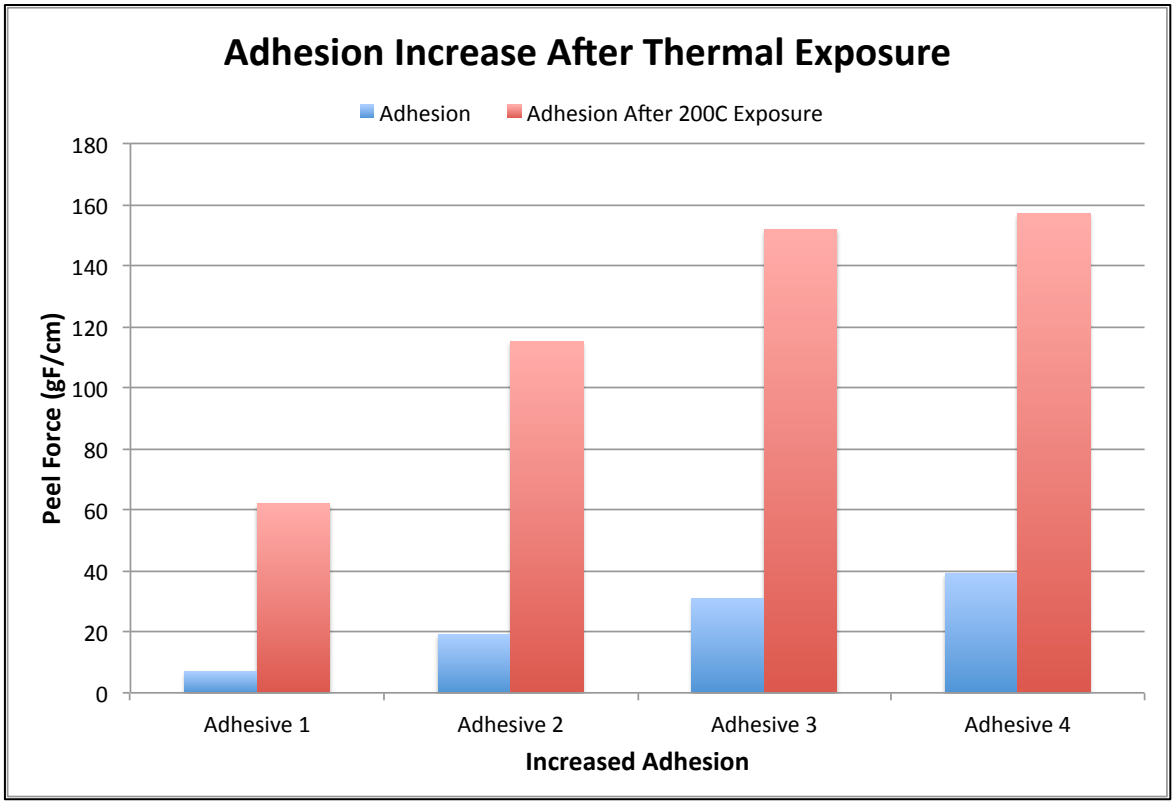
Adhesion vs. Bonding Pressure

- Adhesion force increases with pressure



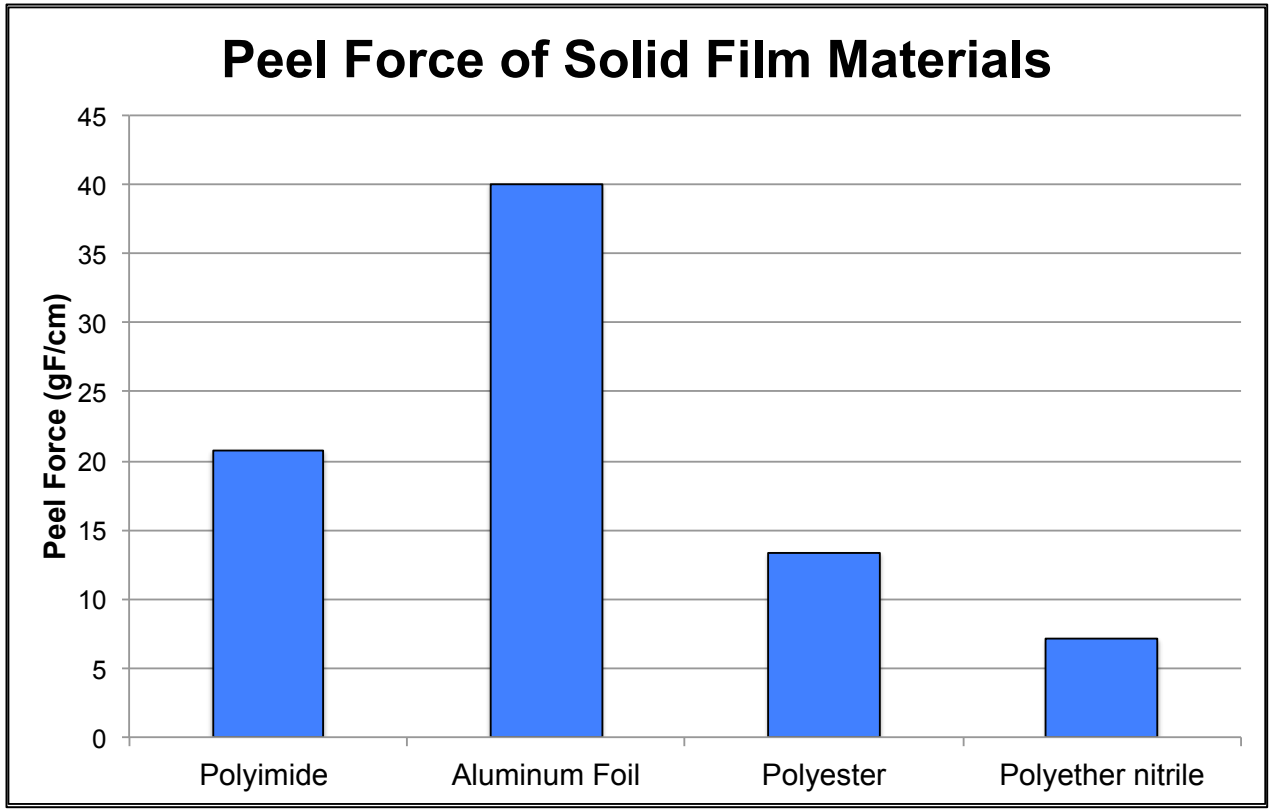
Adhesion vs. Process Temp

- Adhesion force increases with temperature



Adhesion vs. Substrate

- Adhesion force dependent upon substrate



Adhesive Qualities by Application

Application	Modulus	Adhesion	Thermal	Uniformity
Mechanical (e.g. thinning)	↑	↑	↔	↑
Vacuum (i.e. PVD, plasma etch)	↔	↔	Tool dependent	↔
Dielectric cure and/or material anneal	↔	↔	↑	↔

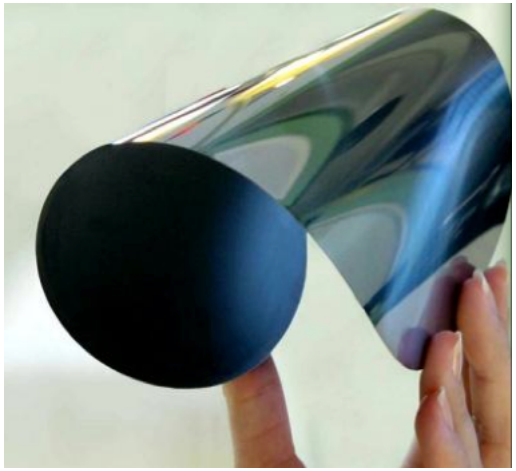
Full process:

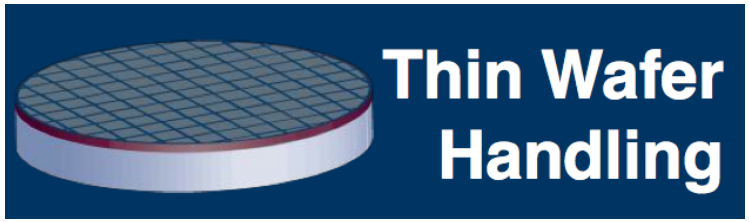
Thinning + backside Process + PI curing	↑	↑	↑	↑
Flexible display (poly-Si anneal)	↔	↔	↑	↑
Pkg EMI Shielding (low temp PVD)	↔	↔	↔	↔

Substrate Characterization

Wafers

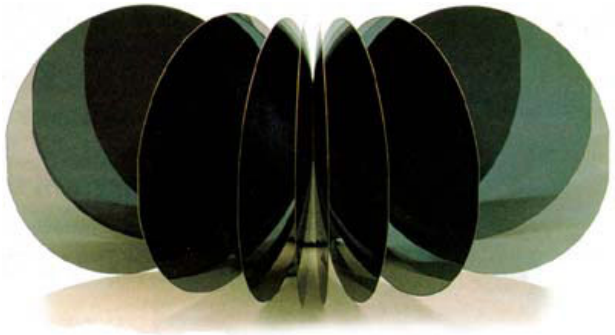
- Wafers thinned to <100um
- Carriers are required
- Debonding generates problems, can be a bottleneck, high cost, and source of yield loss

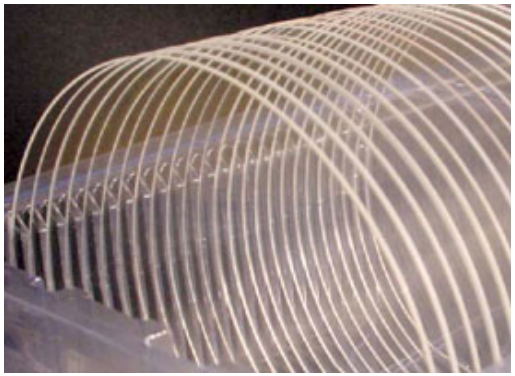




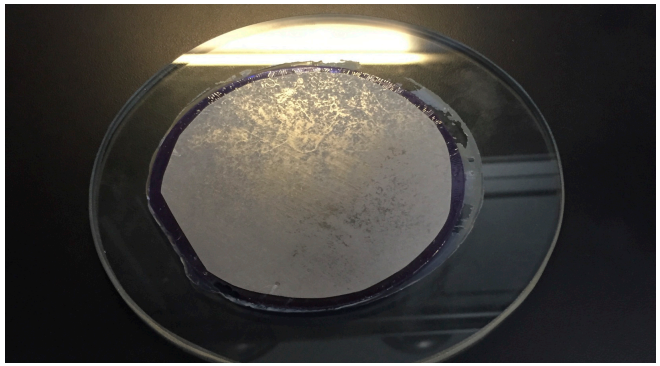
Carriers

- Silicon
- Glass
- Sapphire
- Tape

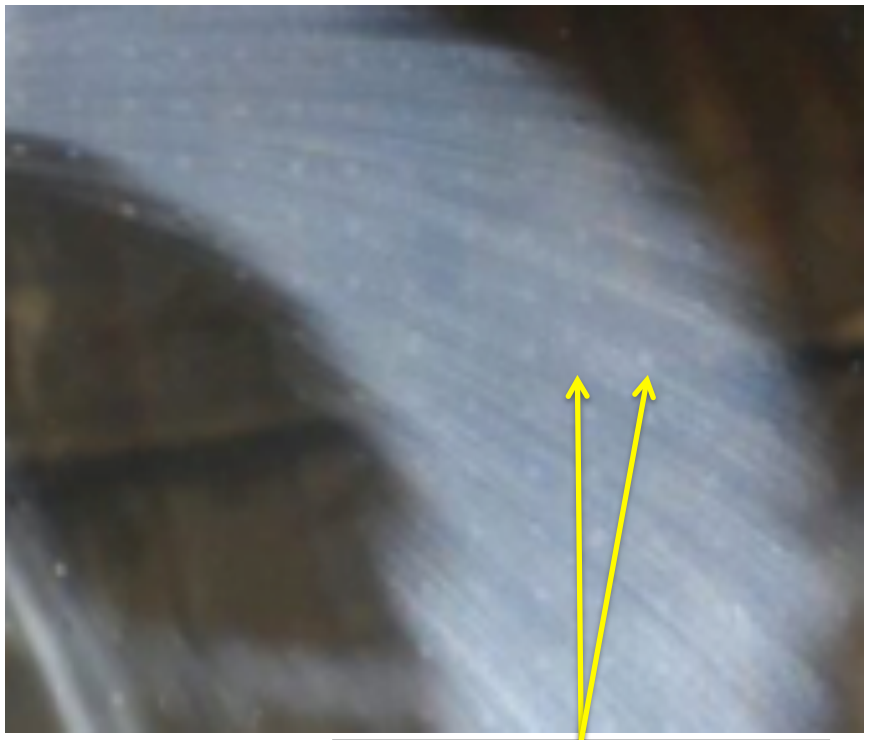




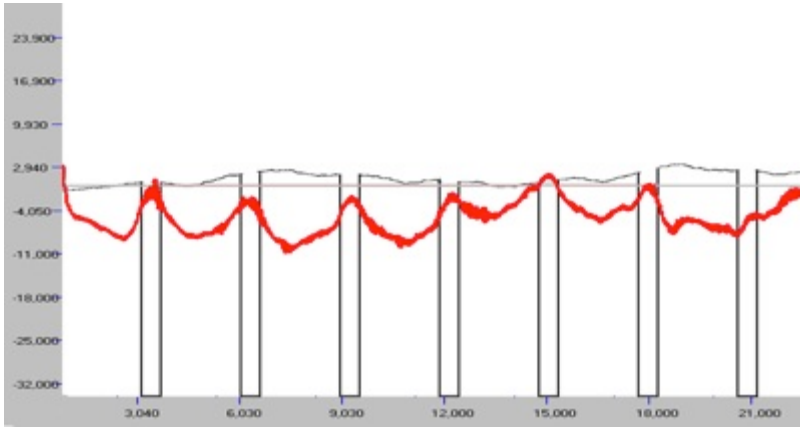
Porous Carriers



Perforated Glass, 50 µm



Divots from glass pores



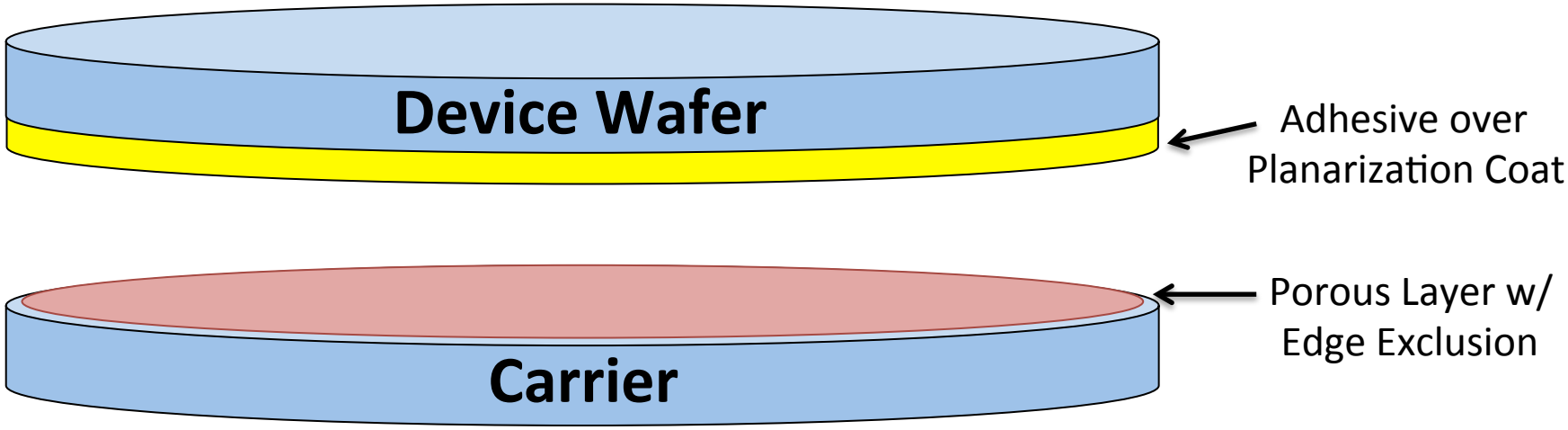
Black: Surface Scan of Perforated carrier
Red: Surface Scan of ground wafer with perforated carrier

Surface Scan shows the divots from glass pores

Porous Carrier

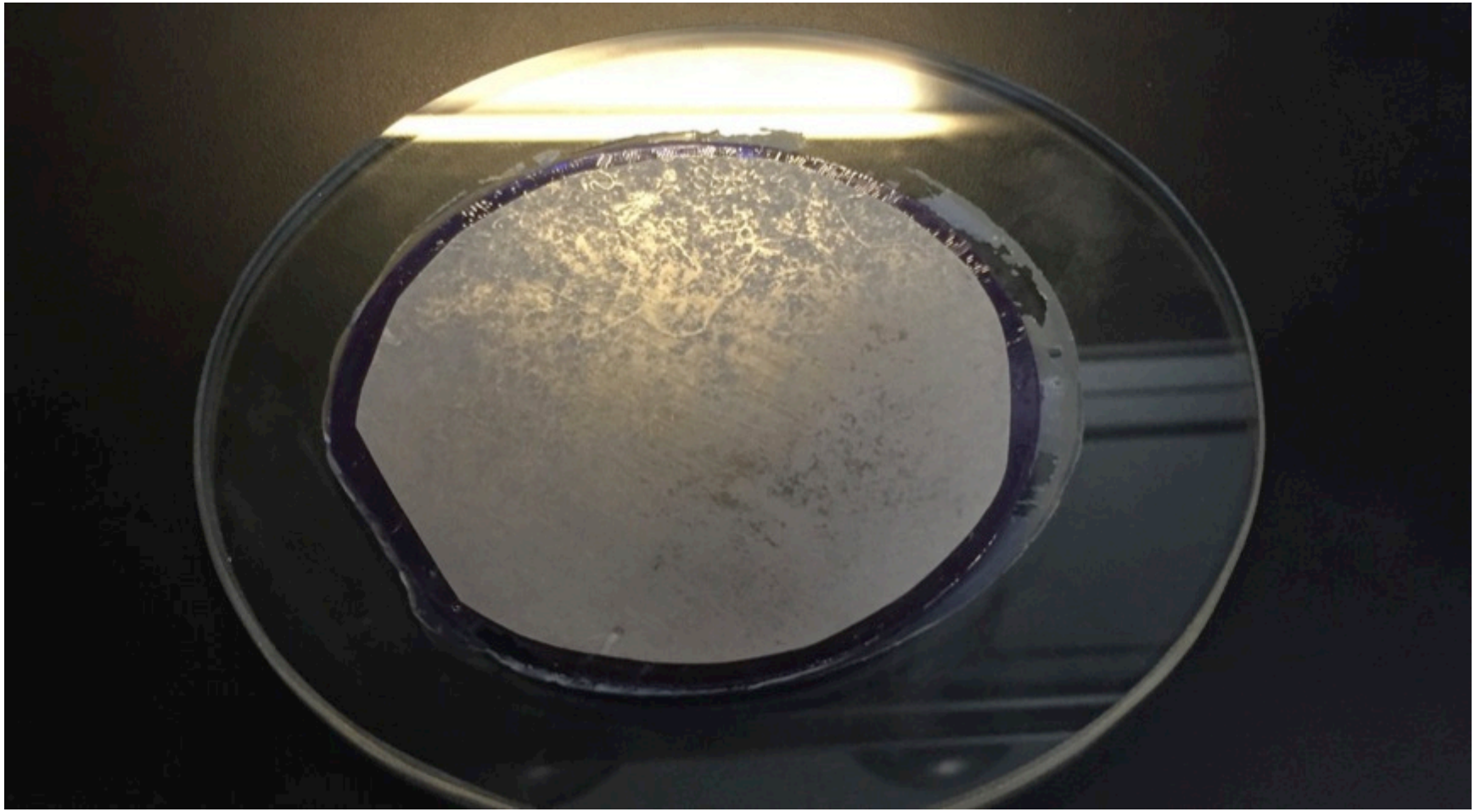
Benefits

- Thermal & chemical resistant
- Simple bond, high adhesion
- Accepts many adhesive types
- Passive debond (chemical diffusion)
- Device wafer on film frame
- Recycle >10X

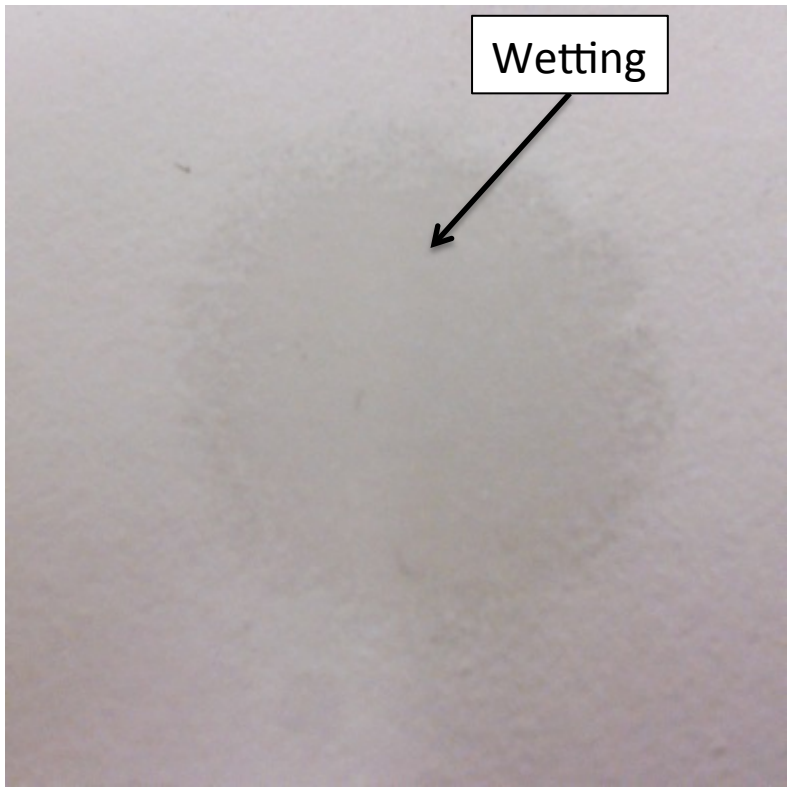


Porous Metal Carrier

Polishing to TTV



Surface Treatment

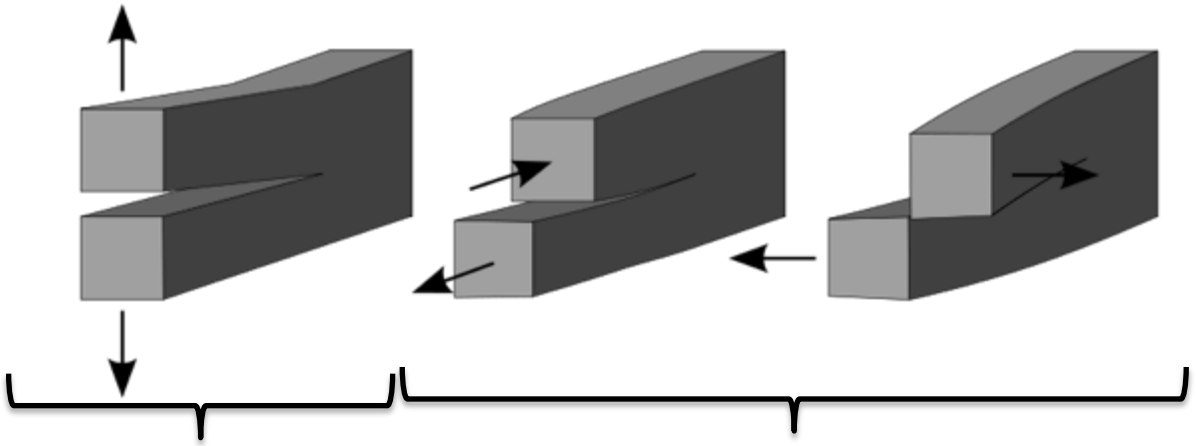


Without Exclusion Layer

With Exclusion Layer

Bonding & Debonding

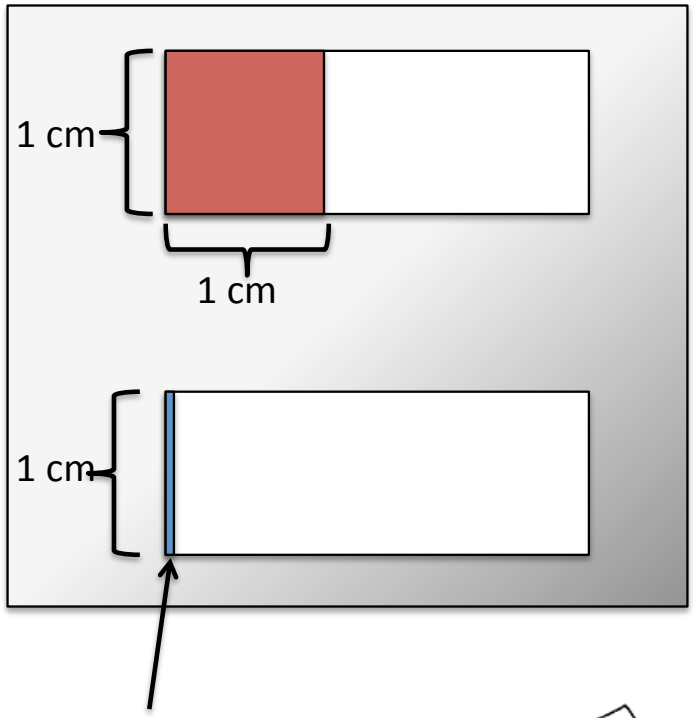
Peel De-bond Mechanics



Common peel separation

Thermal-slide (shear)

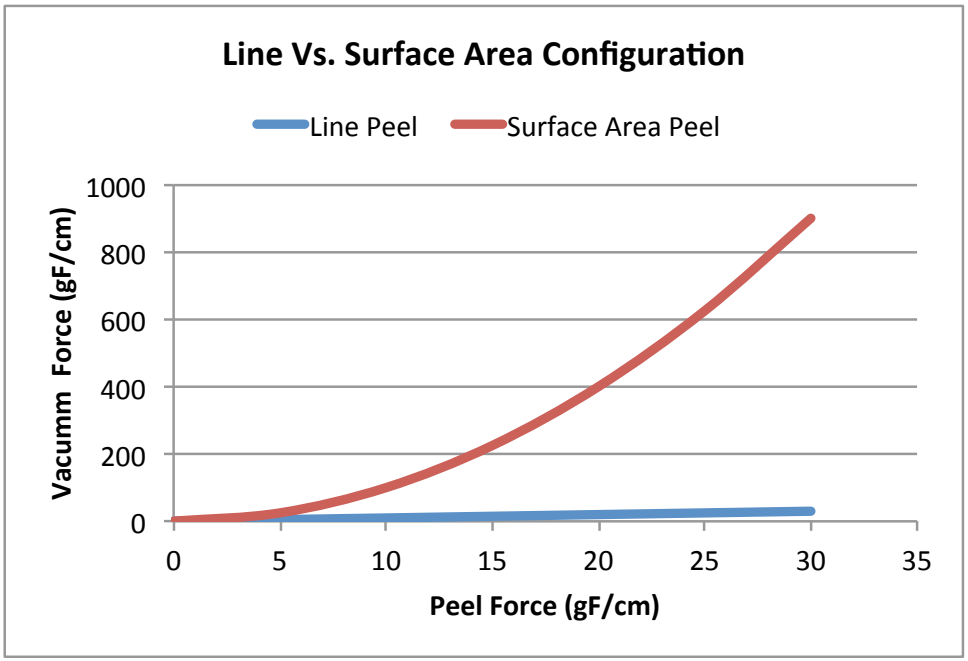
Peel Configurations

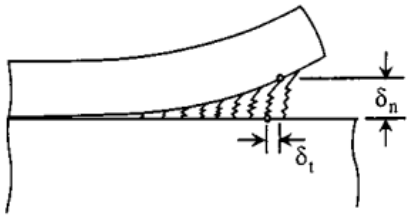


Area Peel

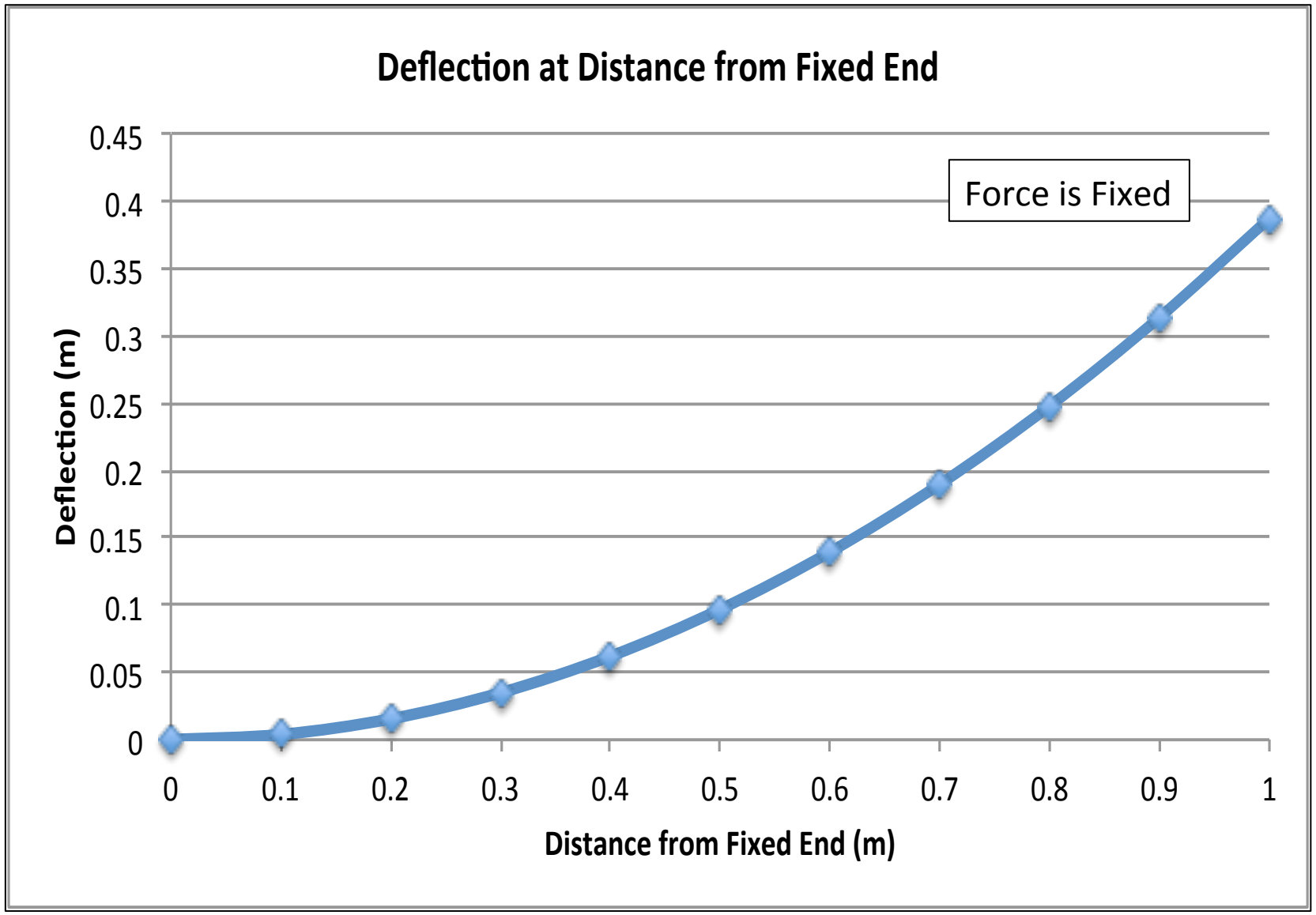
Vs.

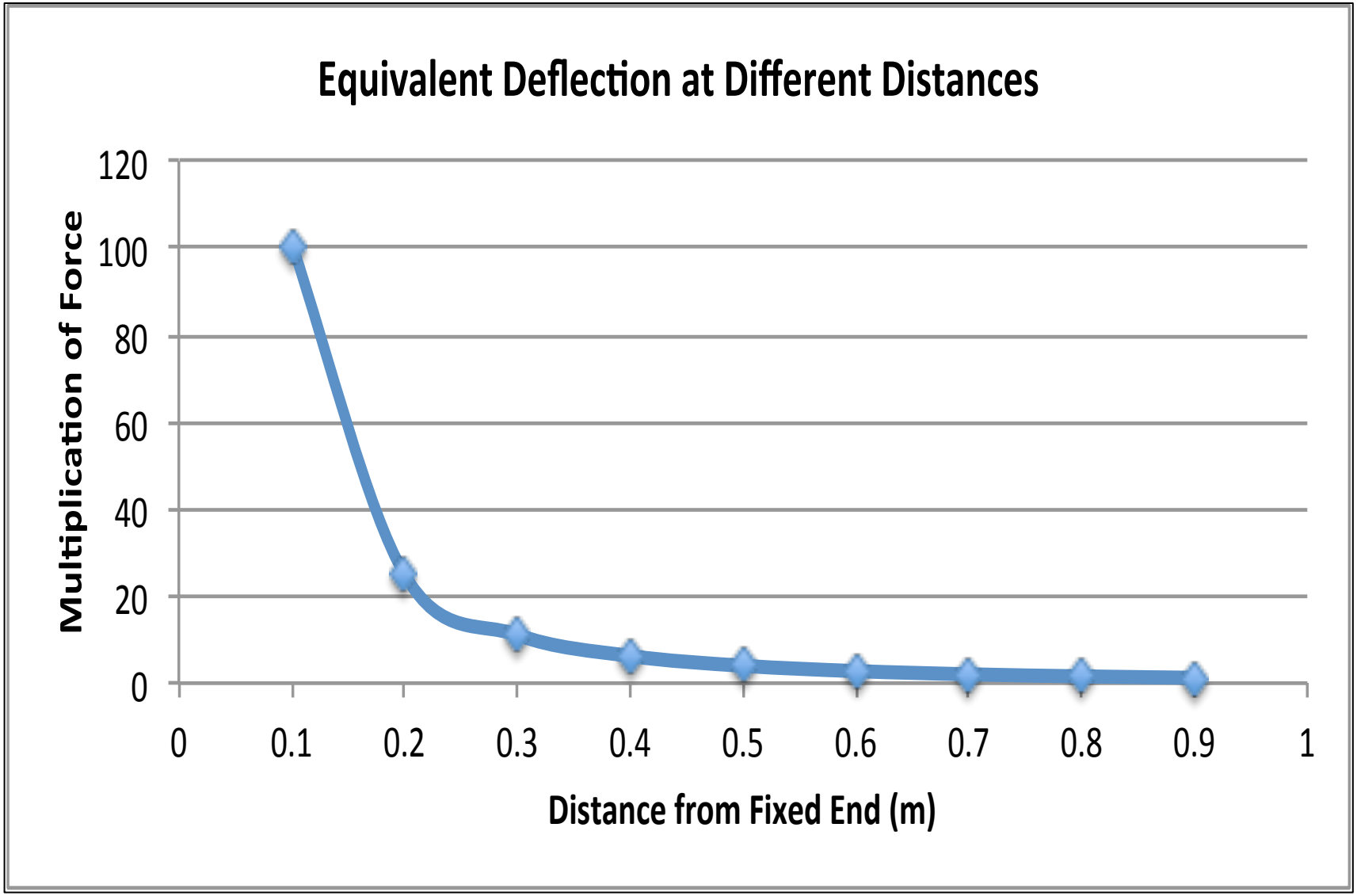
Line Peel



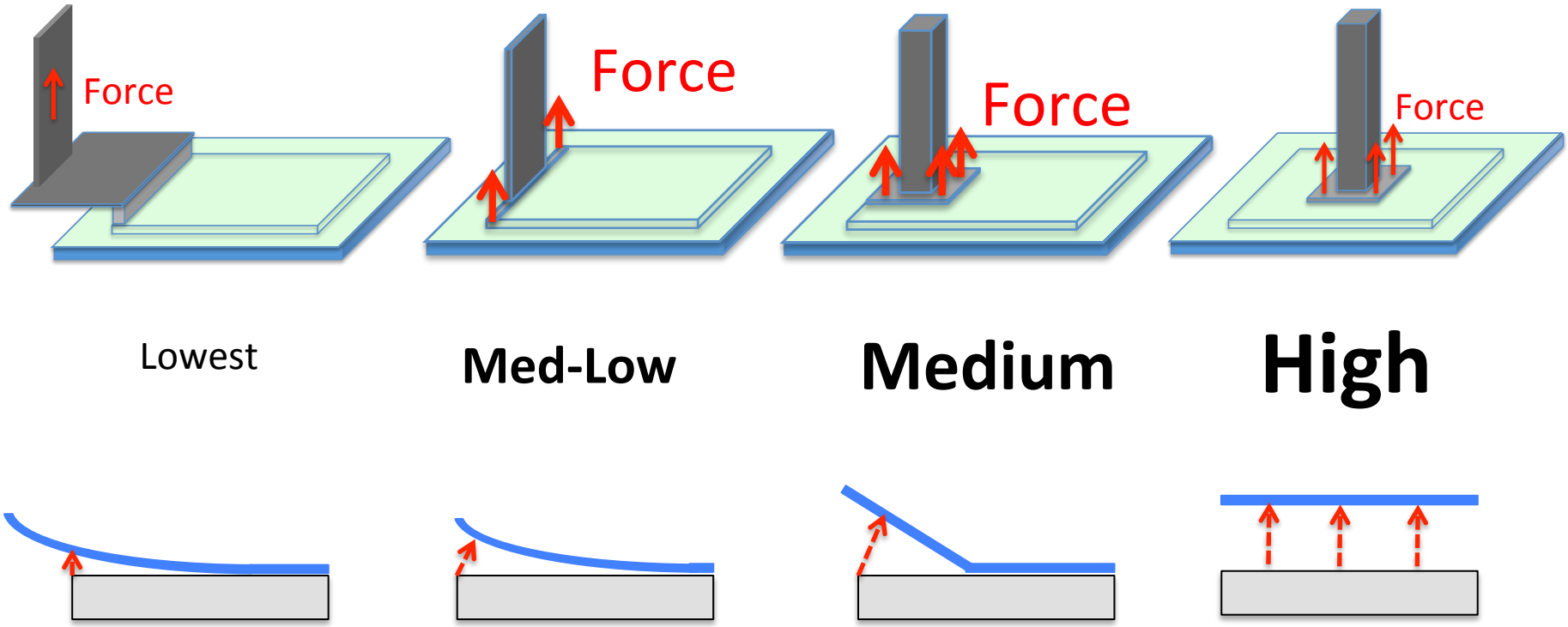


- Line peel separates from adhesive in specific zone
- Adhesion force is lower, shear, and stress

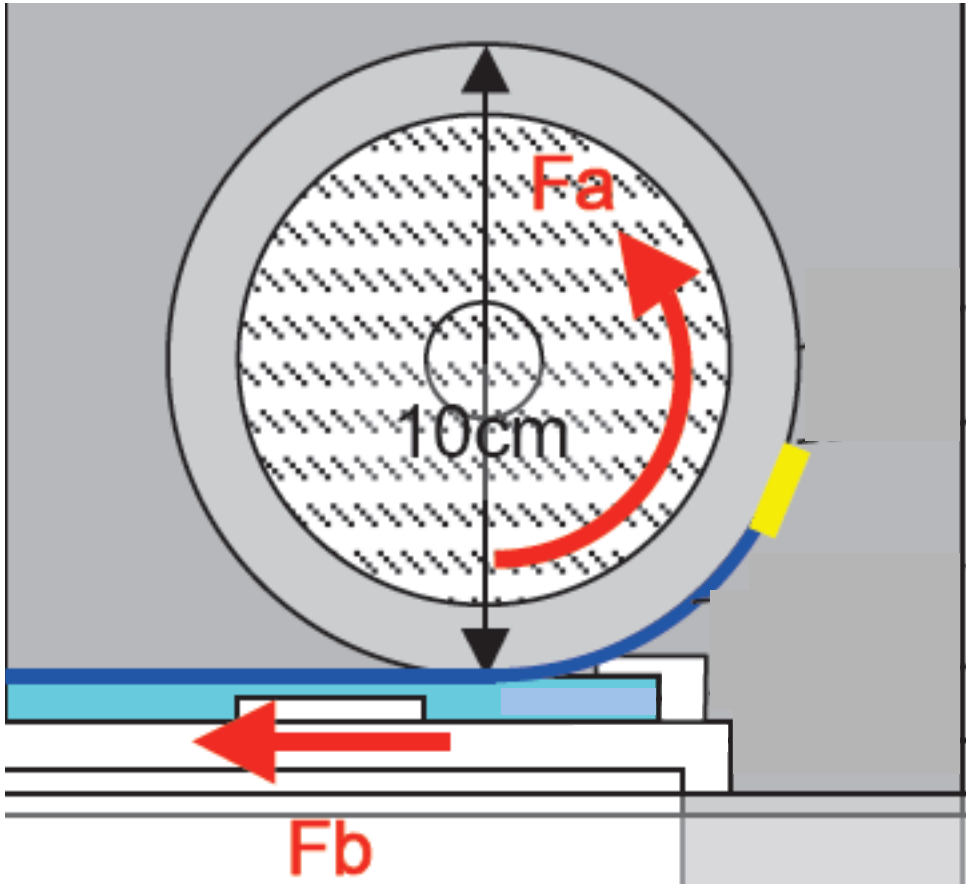

Deflection at Distance from Fixed End
Force is Fixed
Deflection (m)
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Distance from Fixed End (m)


Equivalent Deflection at Different Distances
Multiplication of Force
120
100
80
60
40
20
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Distance from Fixed End (m)

Relative Peel Force

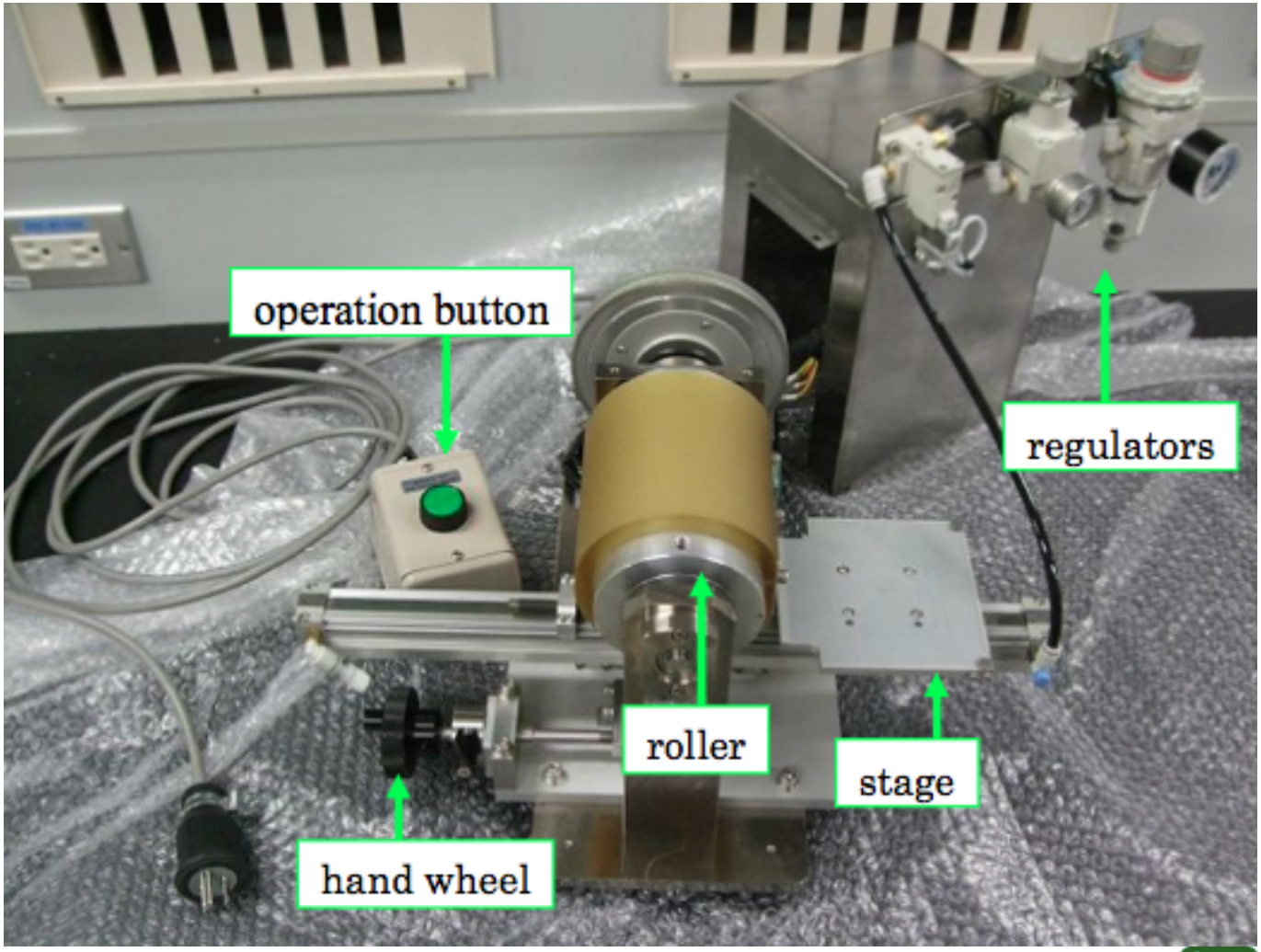


Controlled Adhesion: Roll Peel

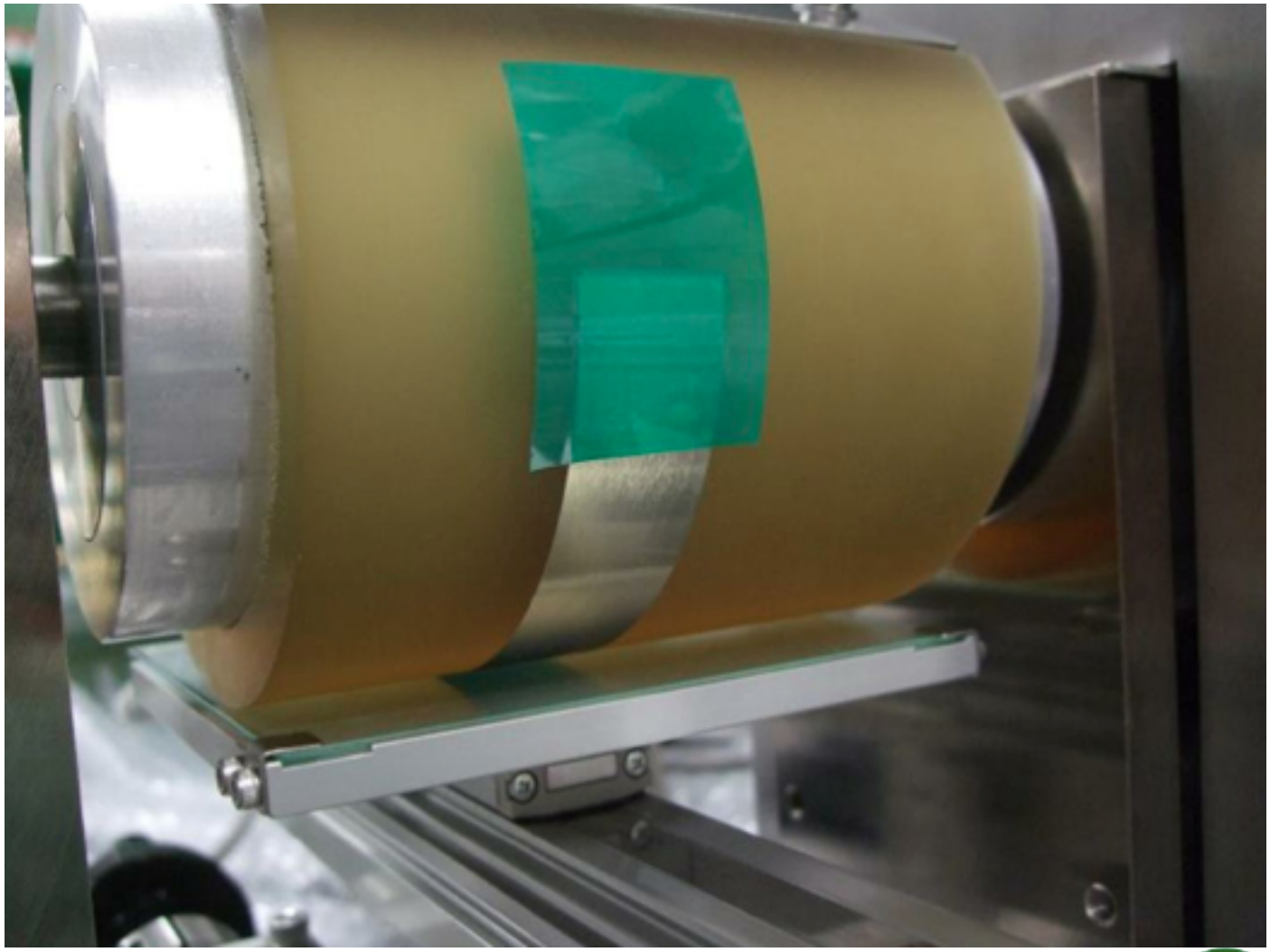


Must Be Custom Equipment

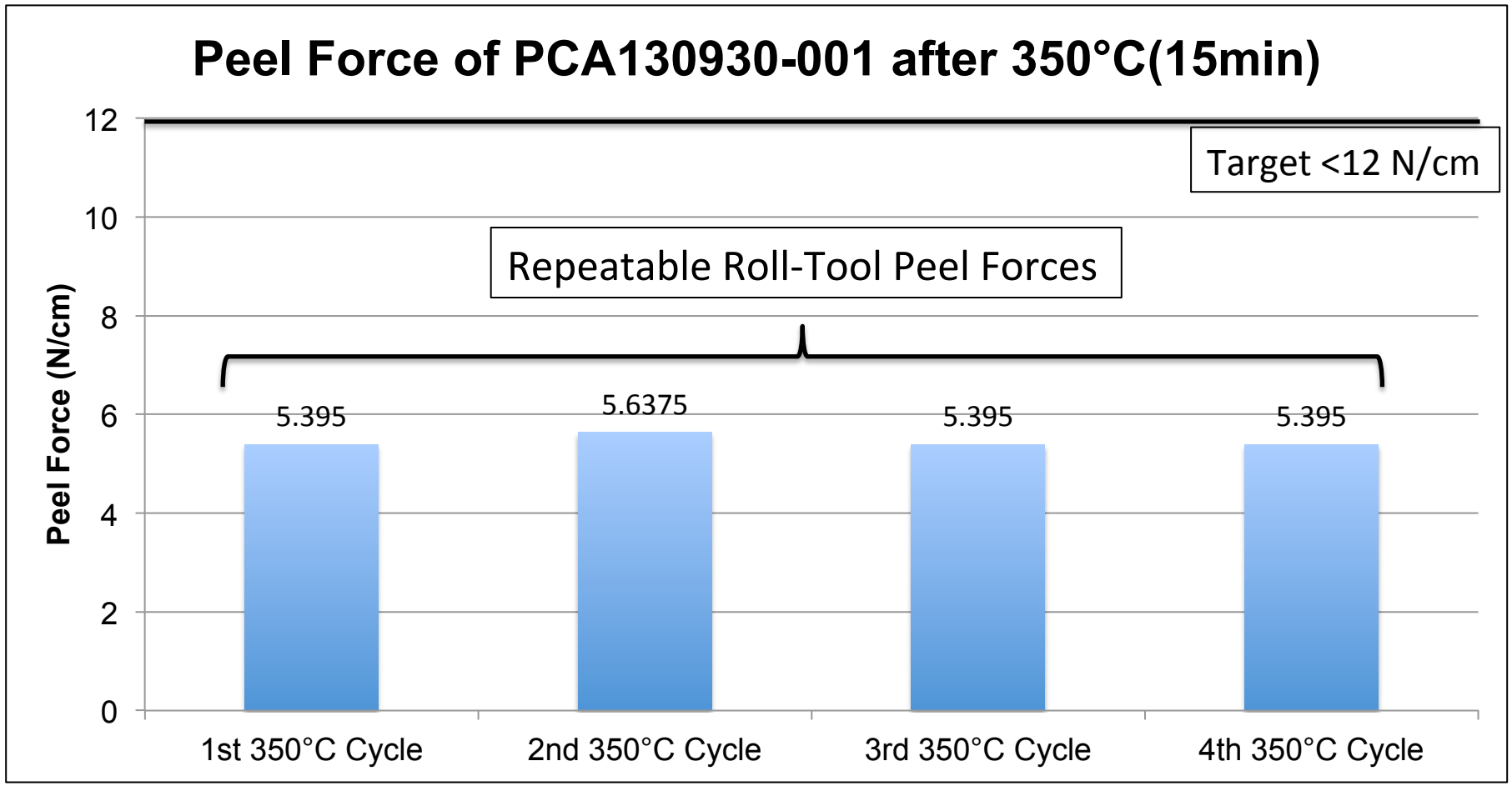
Roll-Tool Mechanics



Performance

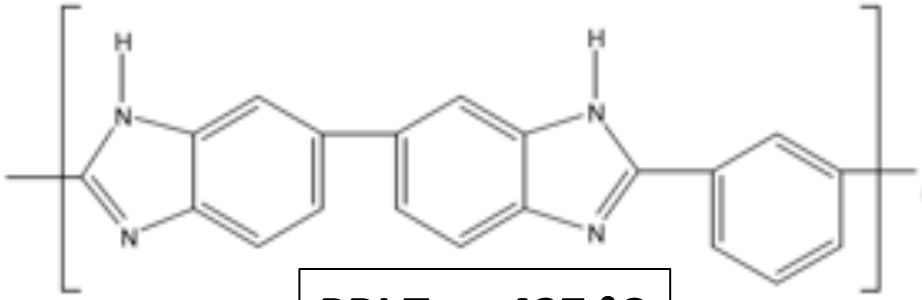


Roll-Tool Repeatability

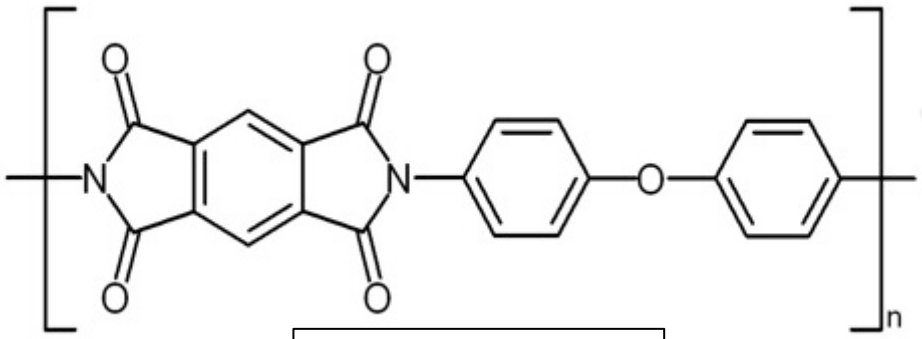


* Cure Program: 150C(10min), 350C (15min) based on TGA Results

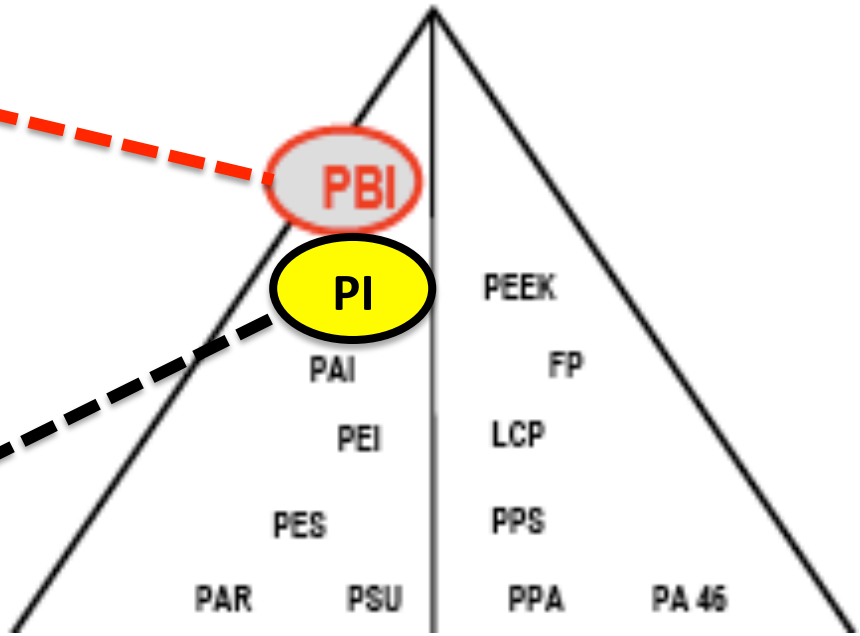
Engineering Polymers



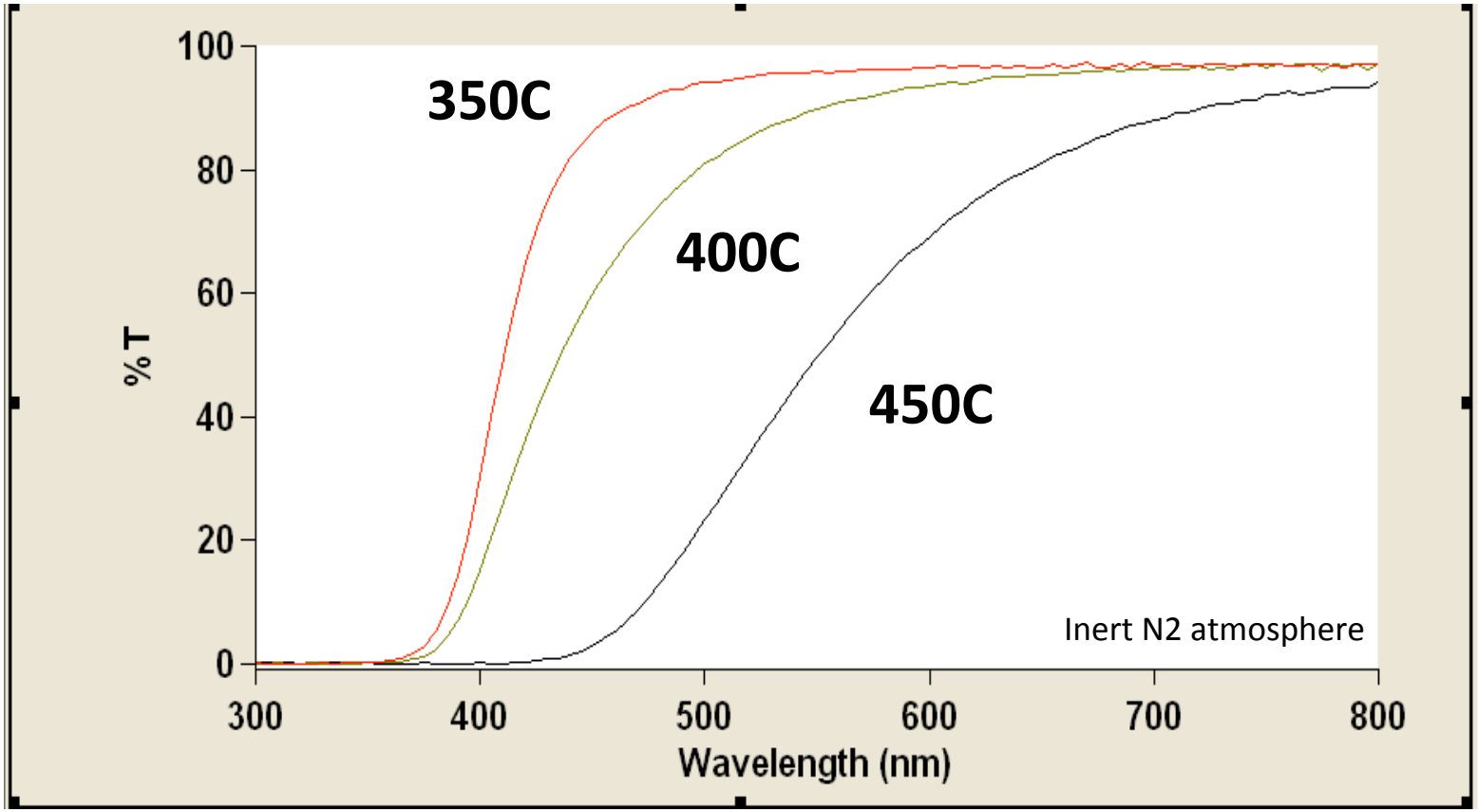
PBI Tg = 427 °C



PI Tg = 370 °C



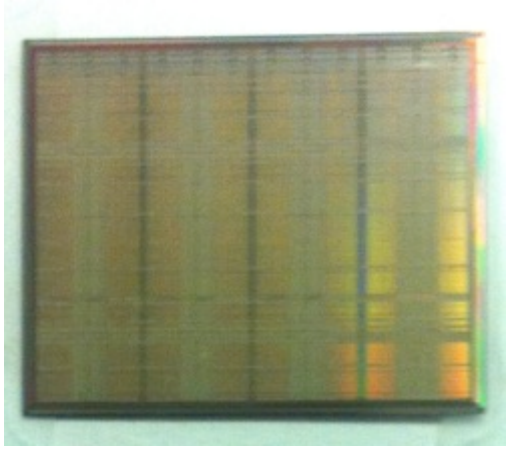
Typical PI Transparency Thermal Trend



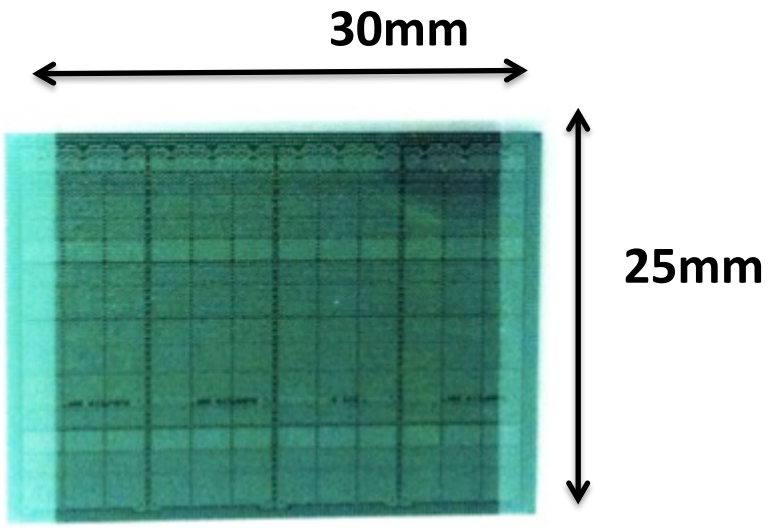
Case Histories

Ex. 1 – Die bond on TSI BGA

- Thin Silicon Interposer (TSI)
- Substrate ~100um thickness
- Underlying bumps ~100um height

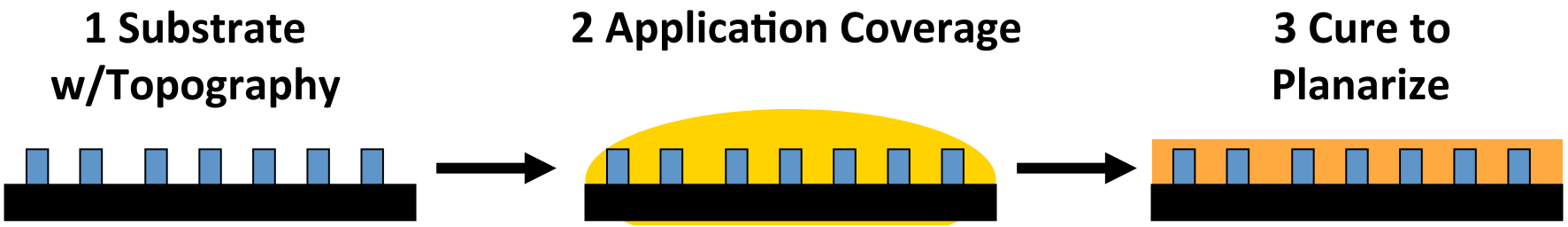


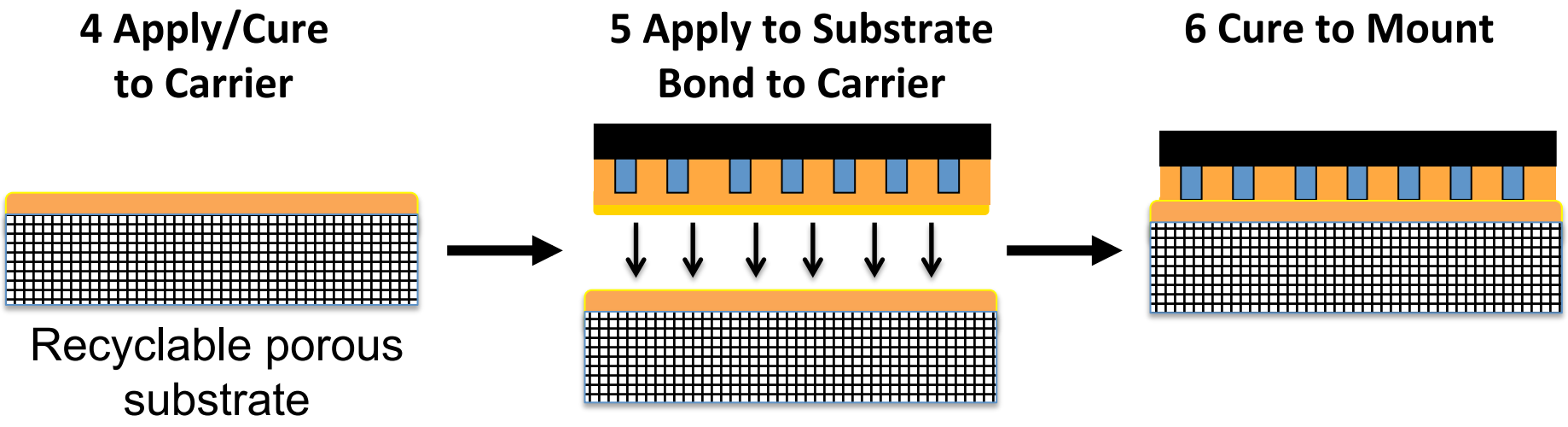
Top side



Bottom side
(contains solder bumps)

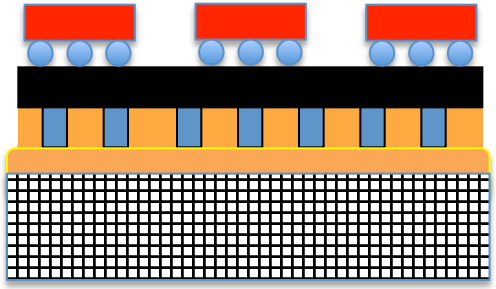
Adhesive Application and Bonding





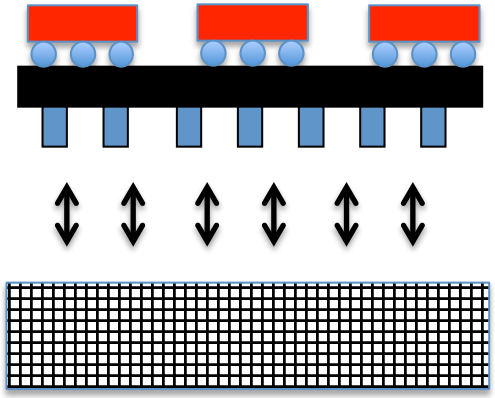
Post-Bonding Process

7 Customer Process



Bonded interposer attach chips to interposer Reflow 250-300C

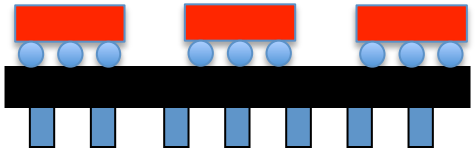
8 Debond & Cleans



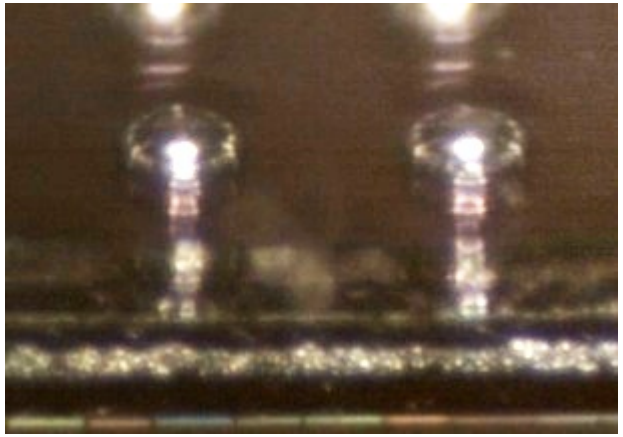
Debond and Cleans rinse, dry

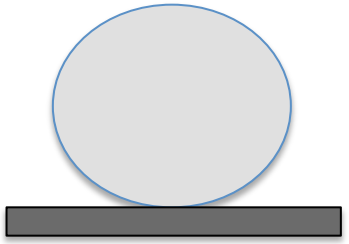
Recycle carrier

9 Acquire Final Product

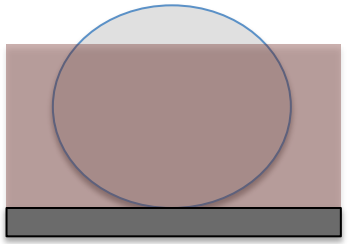


Adhesive Planarization



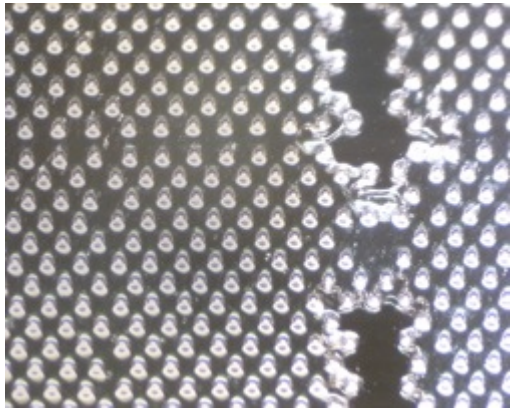


No adhesive

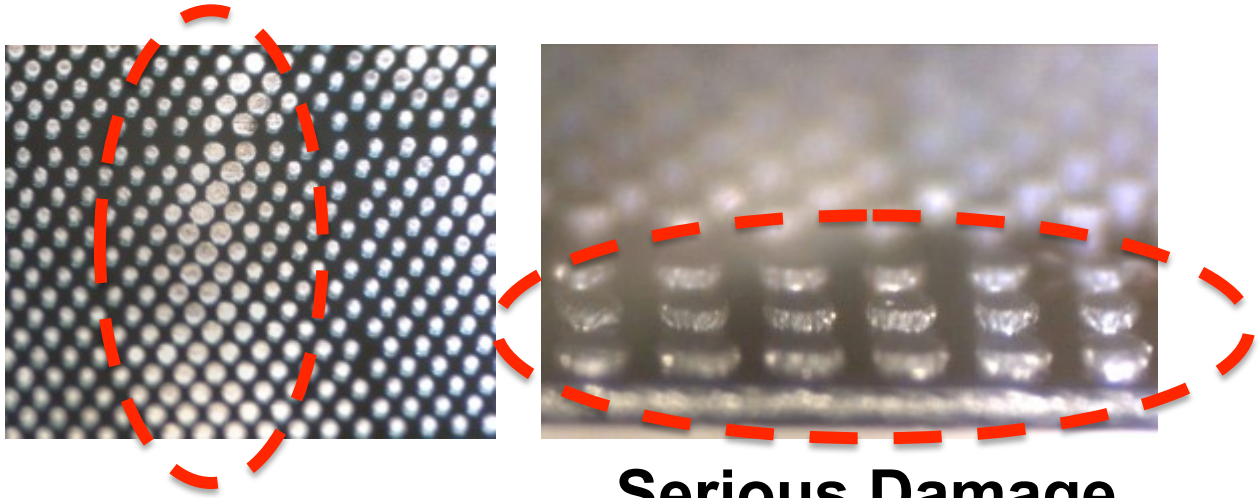


Adhesive

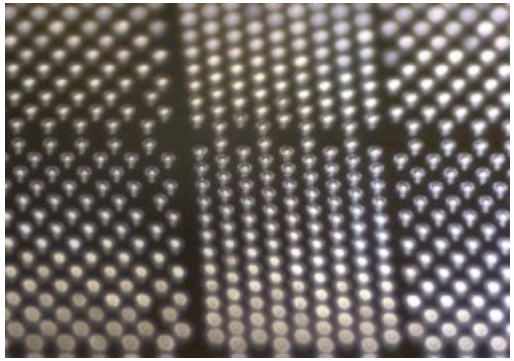
Planarization and Thermal



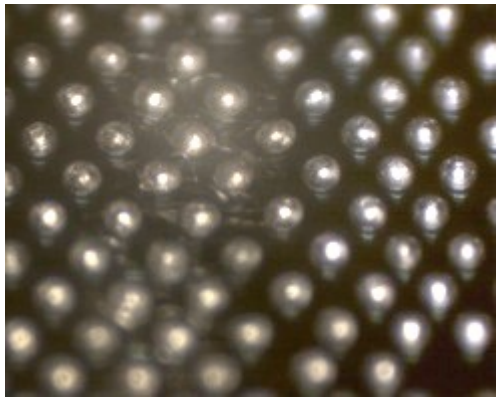
- Voids -



Serious Damage



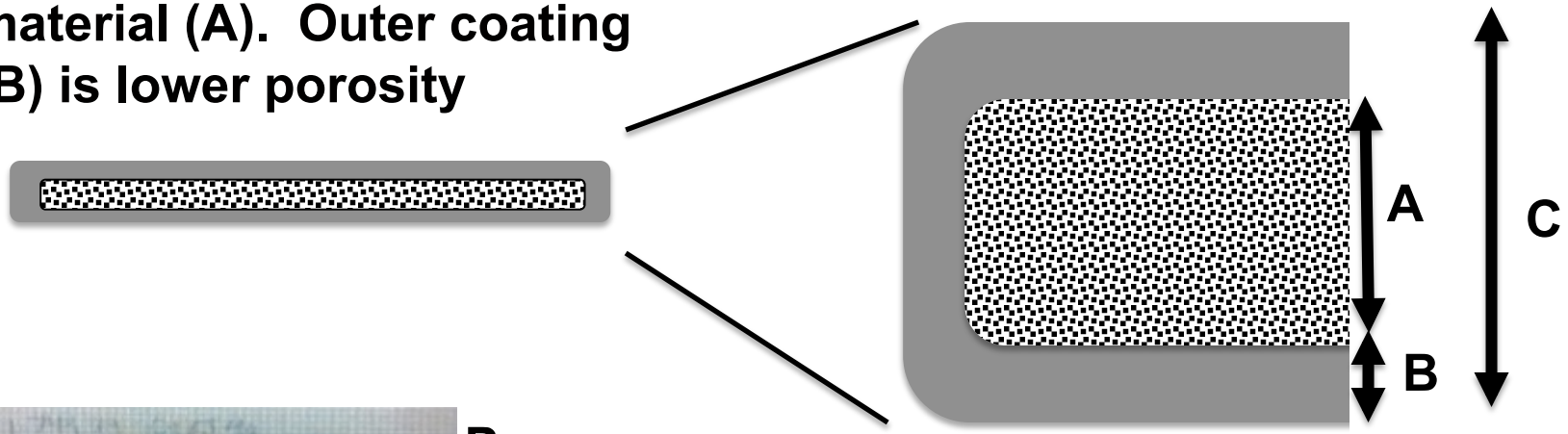
No Voids

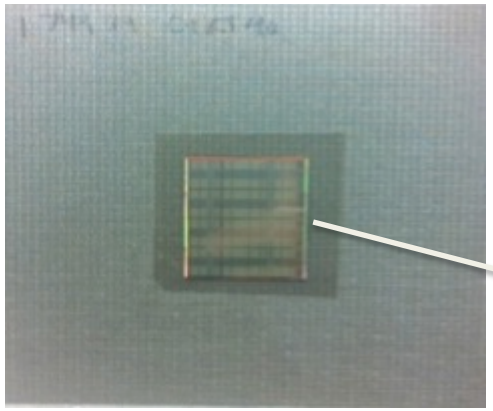


No Damage

Porous Carrier

Porosity higher for inside material (A). Outer coating (B) is lower porosity



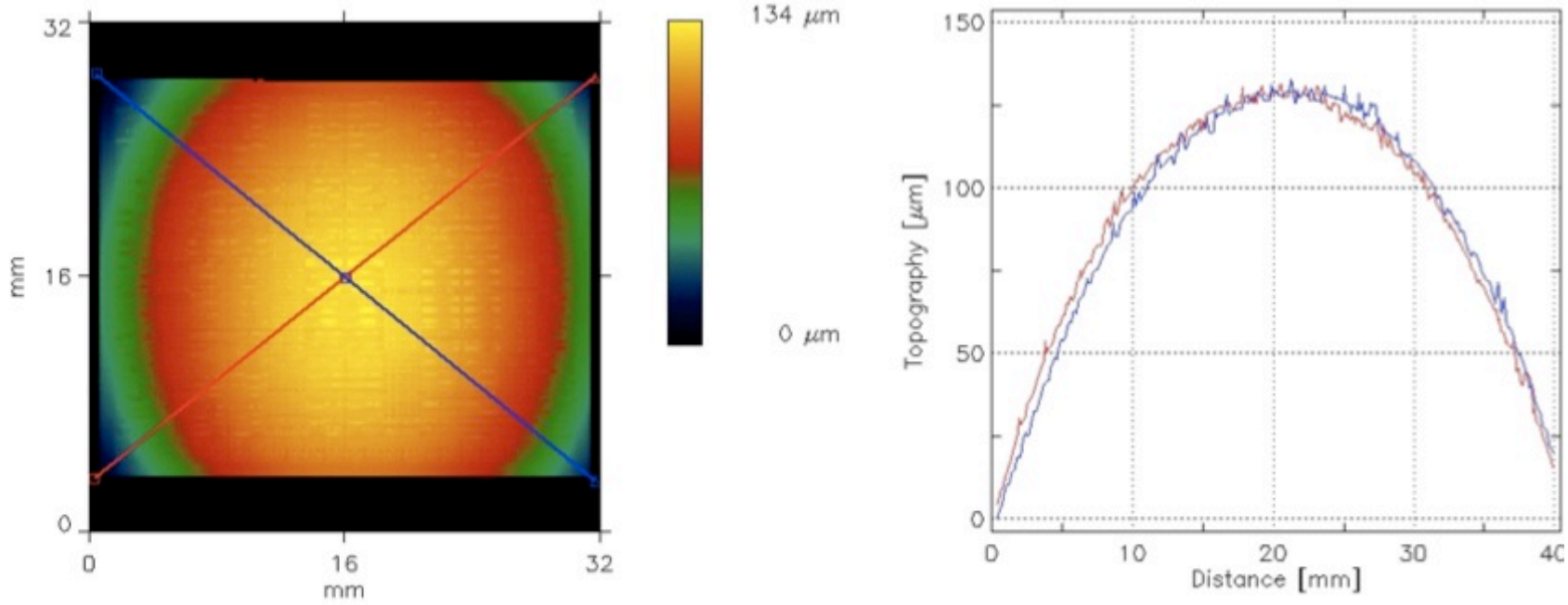


Porous Carrier

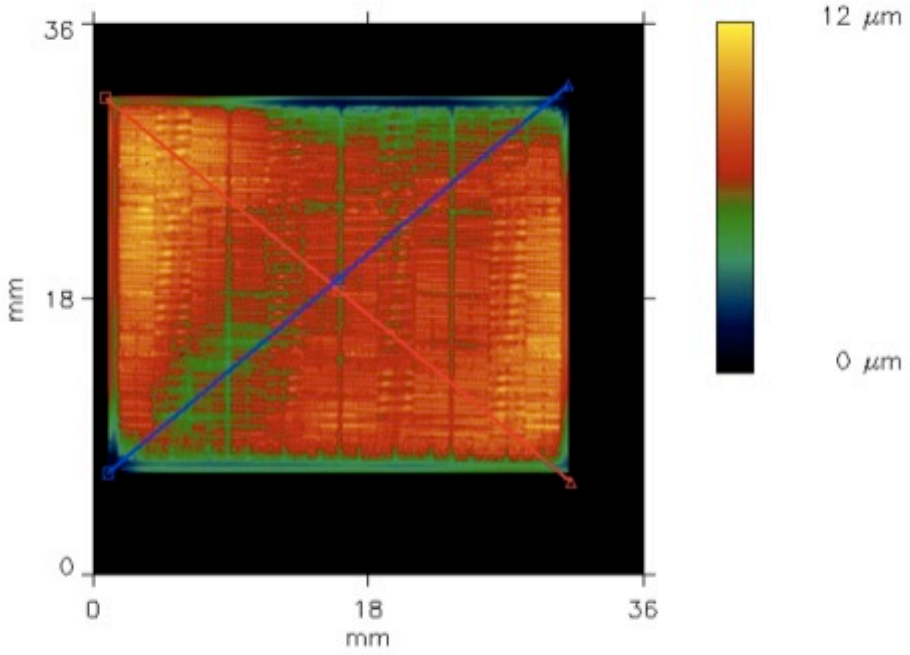
TSI on adhesive

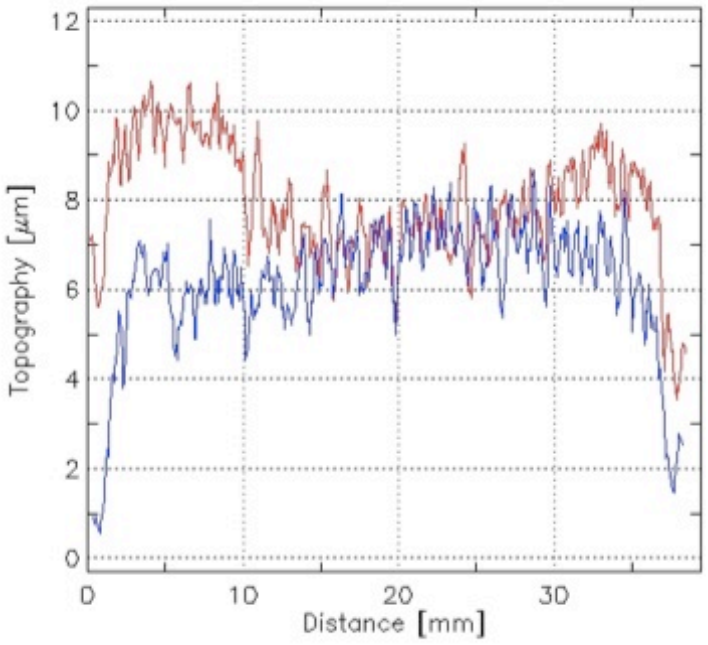
A = 0.5 – 0.8mm
B = 0.1 - 0.25mm
C = 0.5 – 1mm

Results – baseline TSI

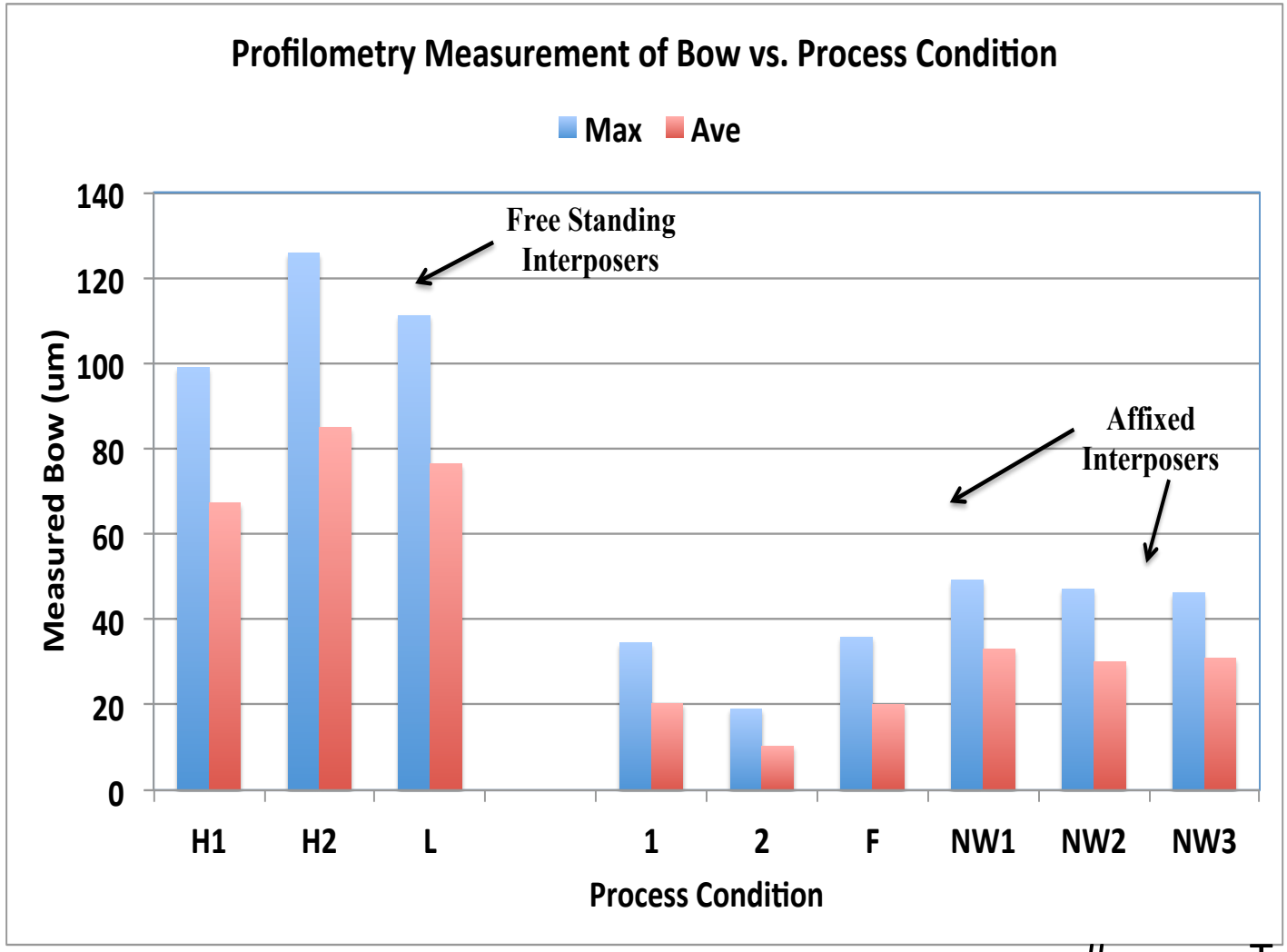


Results – Bonded TSI

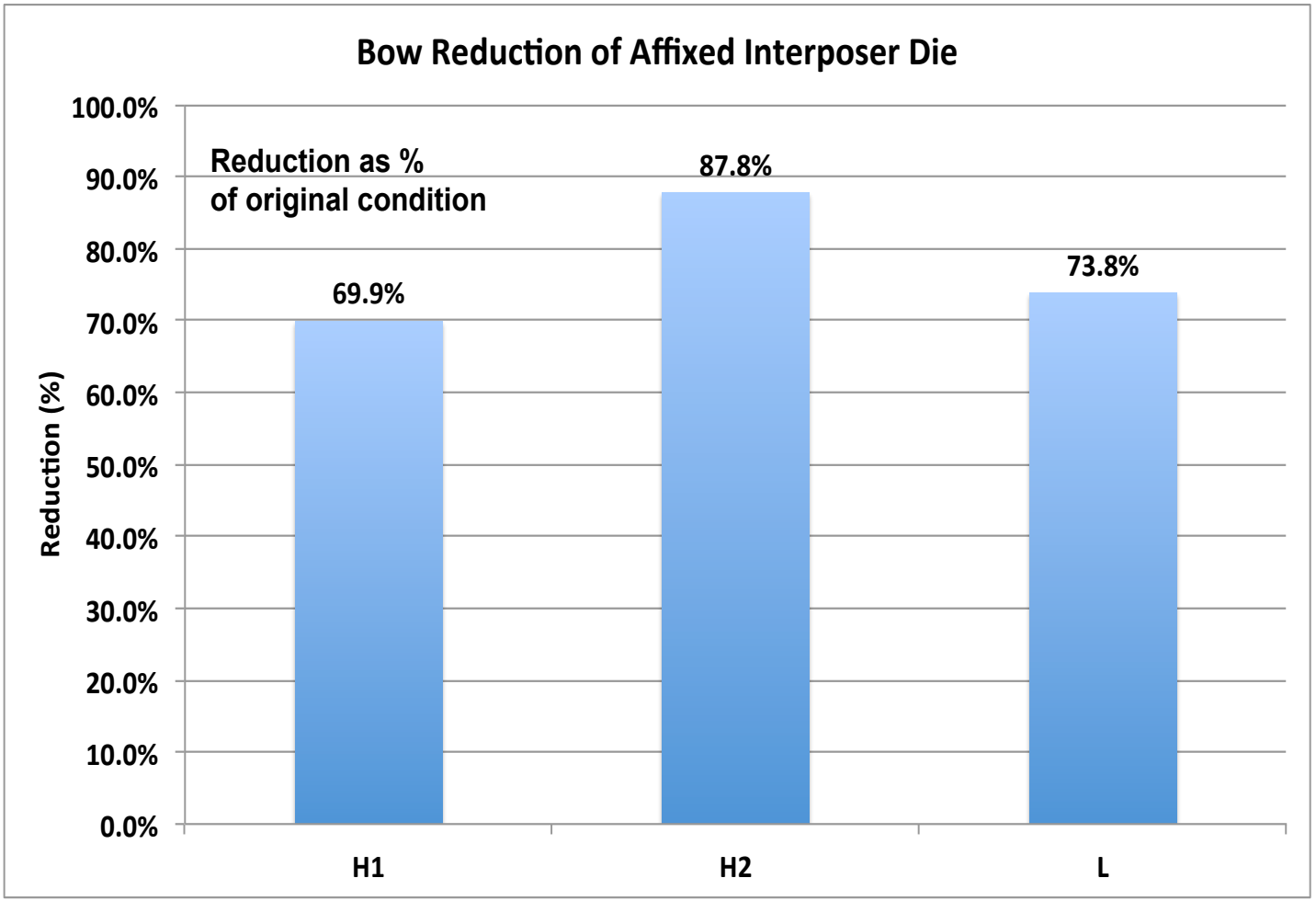




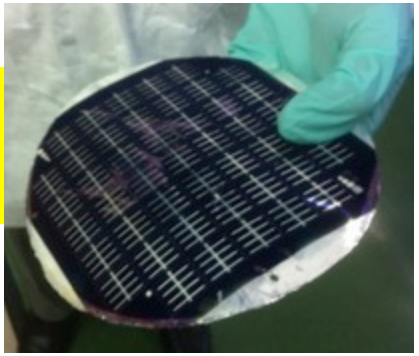
Variation <12um

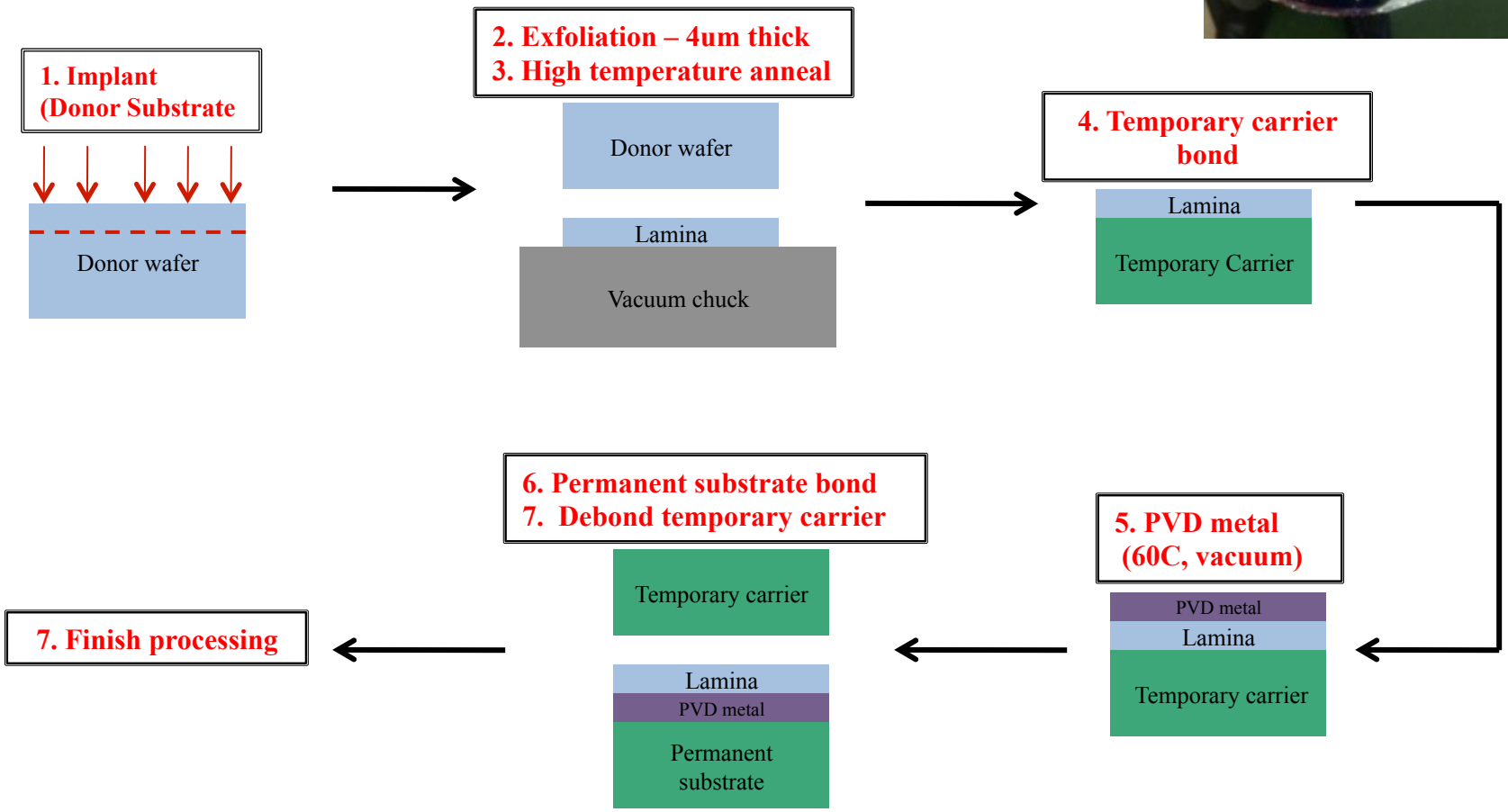


#	Type
1, 2, F	Peripheral
NW	Porous Subst


Bow Reduction of Affixed Interposer Die
Reduction as %
of original condition
Reduction (%)
100.0%
90.0%
80.0%
70.0%
60.0%
50.0%
40.0%
30.0%
20.0%
10.0%
0.0%
69.9%
87.8%
73.8%
H1
H2
L

Ex. 2 – Wafer support (solar)

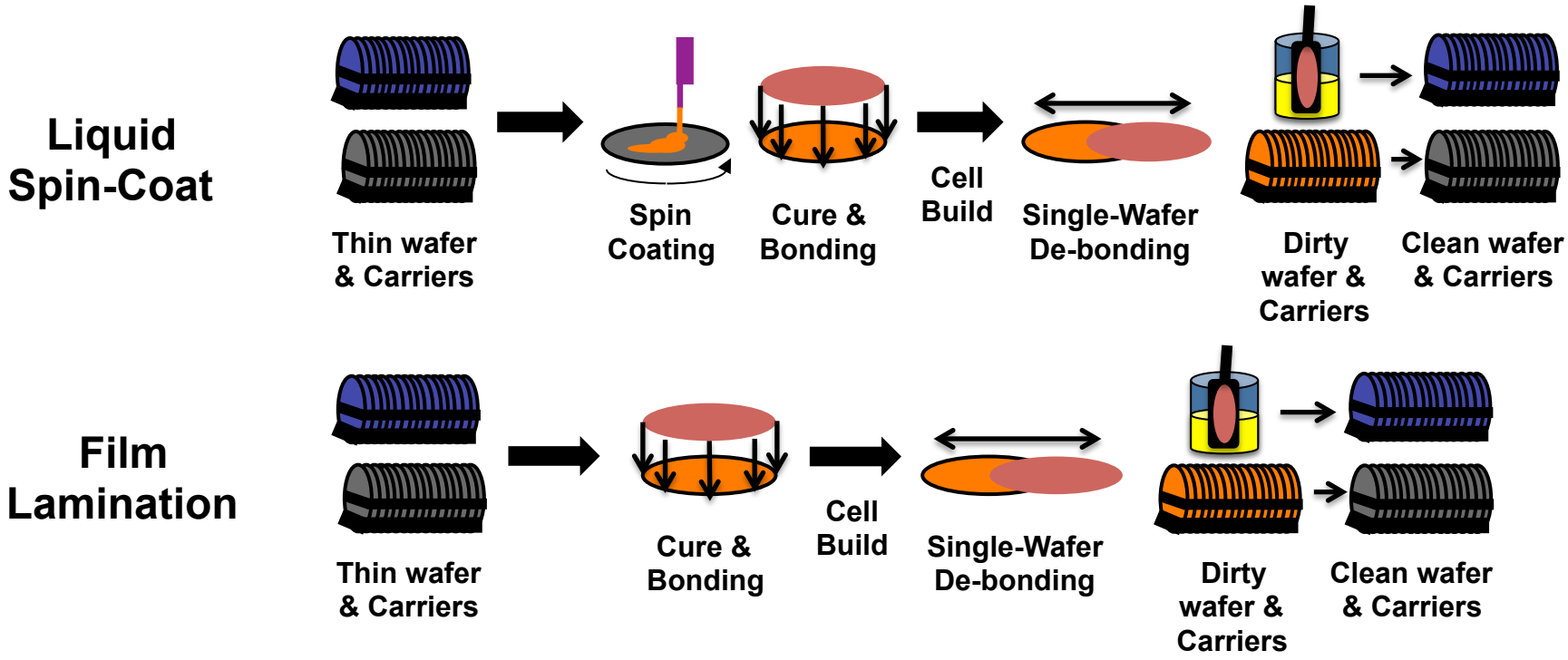




Temporary Bond – Solar

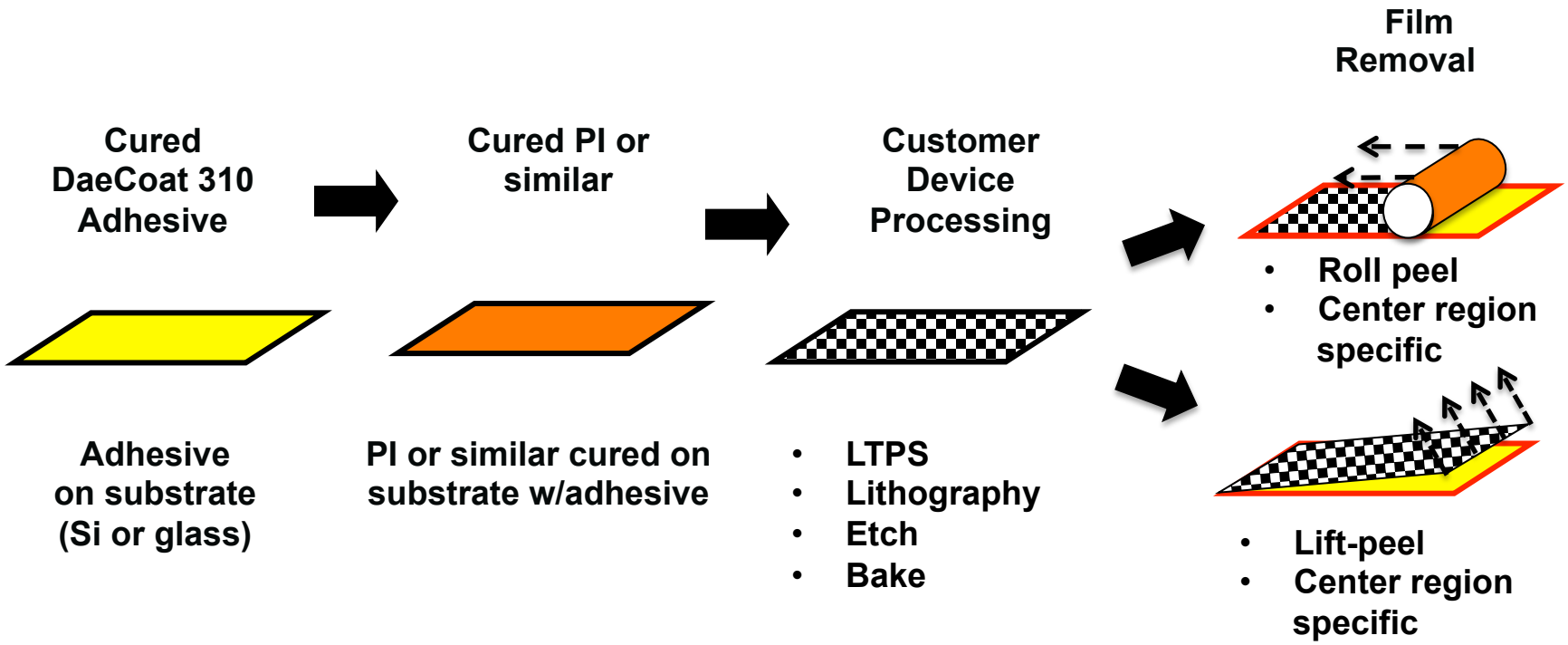
- 4um thin wafer
- Urethane thermoplastic
- Liquid adhesive – proof of concept, complete process development, tooling
- Film adhesive, converted/stamped, roll-to-roll operation on a panel operation

Liquid Conversion to Film



Ex. 3 – Curved Display

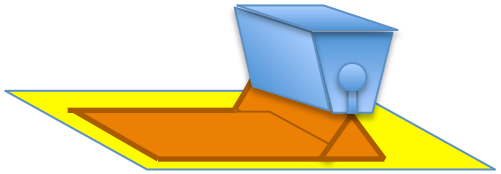
- Cast liquid PI substrate
- Adhesive cured on glass carrier
- Lift-off/peel force tuned for HVM needs



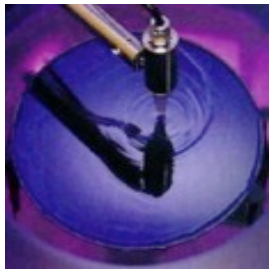
PI or Similar Coating

Daetec's Polyimide

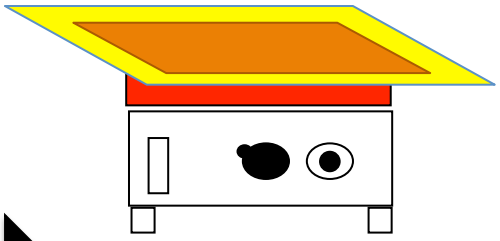
Cured
DaeCoat™ 310



Slit Coating:
1. Adjust Gap height (10-40μm)
2. Apply



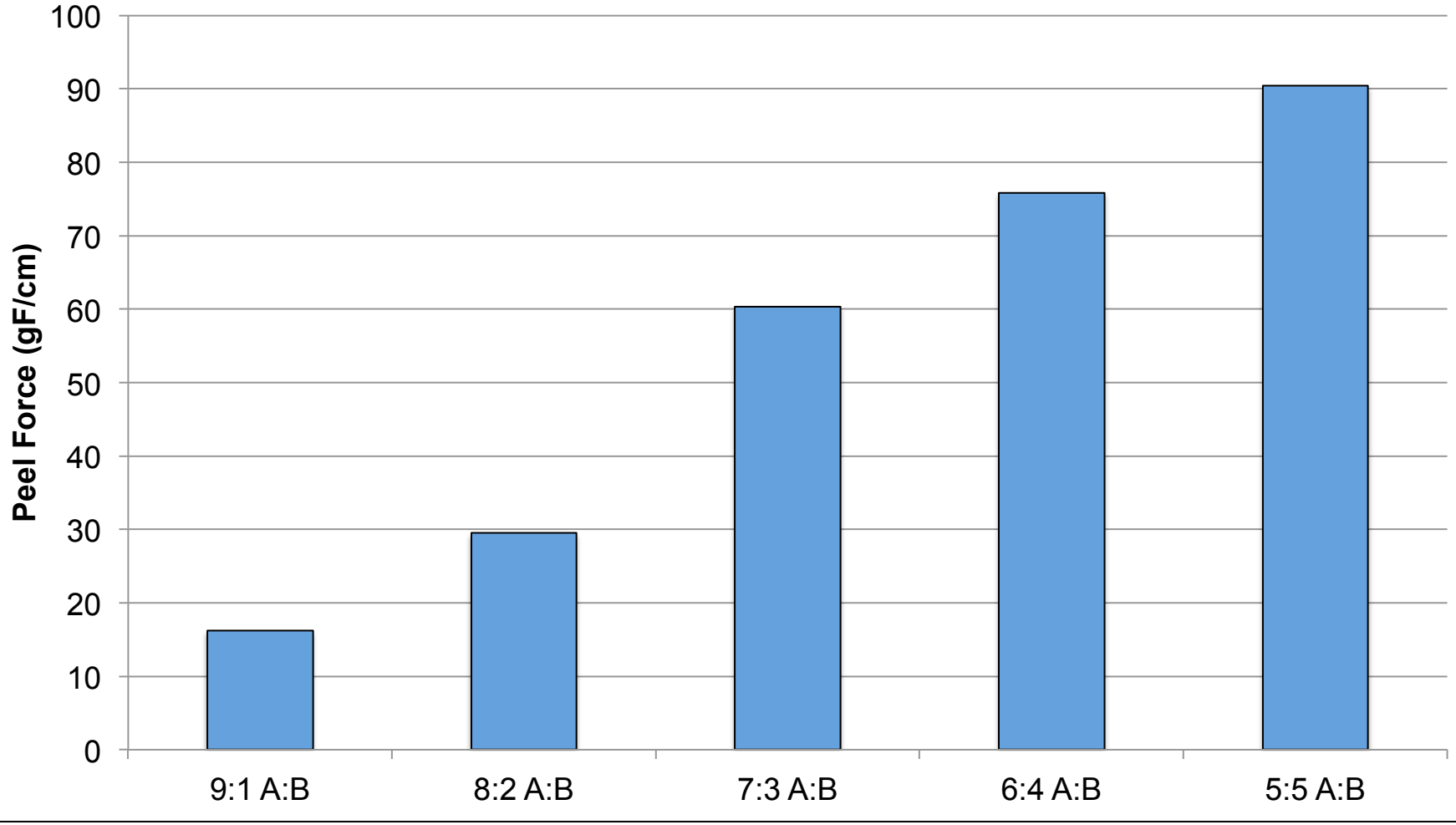
Spin Coating:
1. Dispense
2. 1000-2000rpm (60sec)



(Hot Plate)

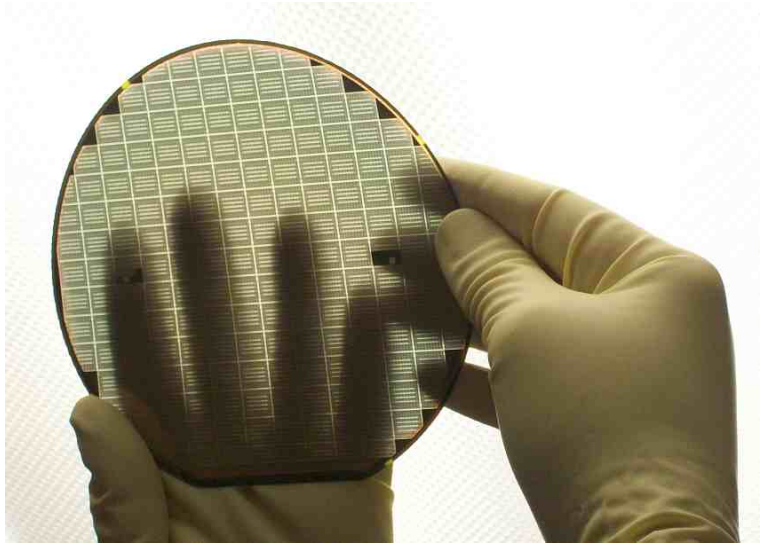
Curing
1. 150°C (5min)
2. 250°C (15min)
3. 350°C (10min)

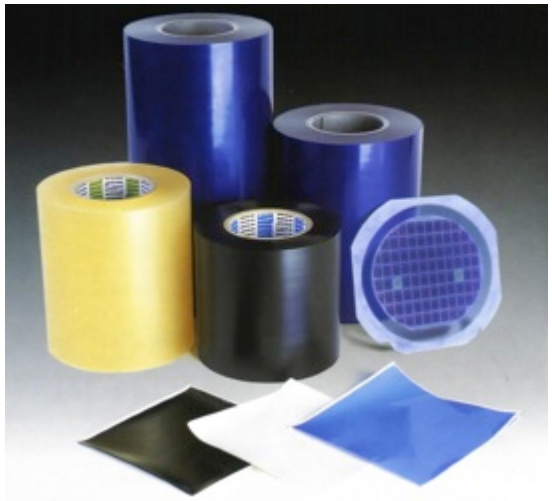
Adhesive Force of DaeCoat™ 315 With Daetec's PI

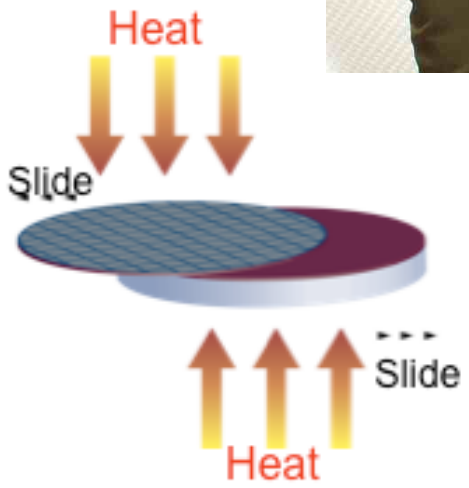


Typical Thin Substrate Support

- Tape
- Vacuum Chuck
- Carrier & Adhesive

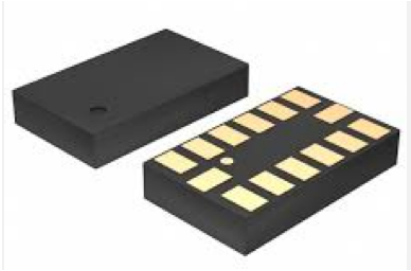




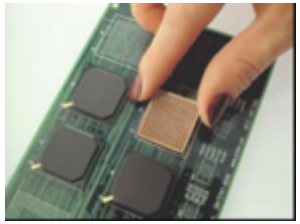


Ex. 4 – EMI Shielding on Devices

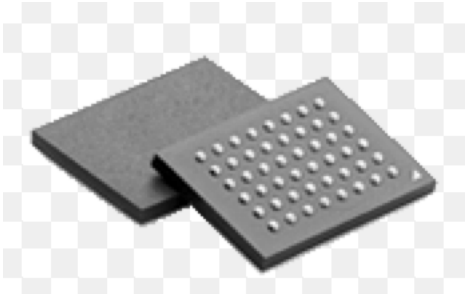
- Cast liquid PI substrate
- Adhesive cured on glass carrier
- Lift-off/peel force tuned for HVM needs



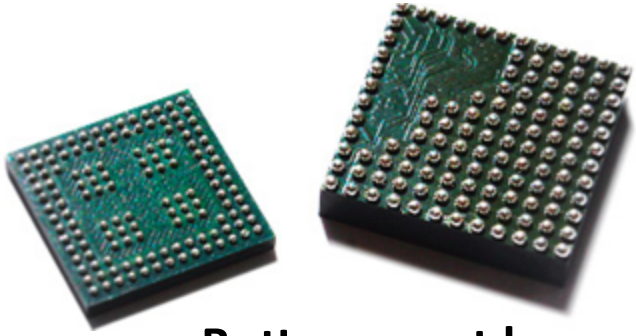
LGA (flat metal pads)



Size 25 X 25mm



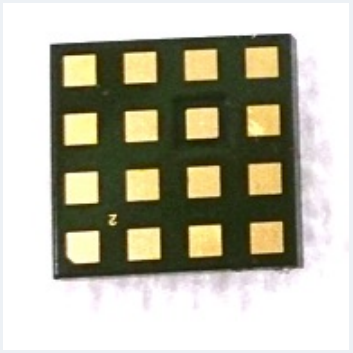
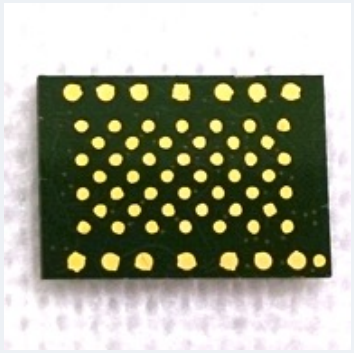
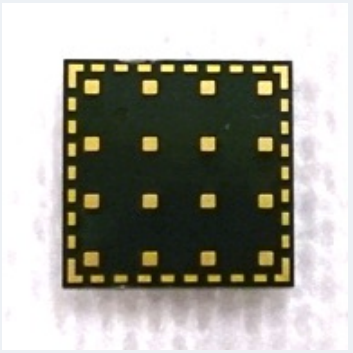
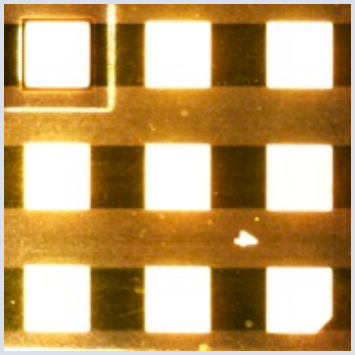
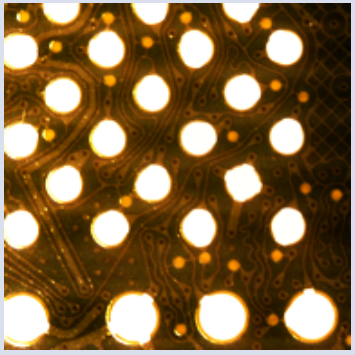
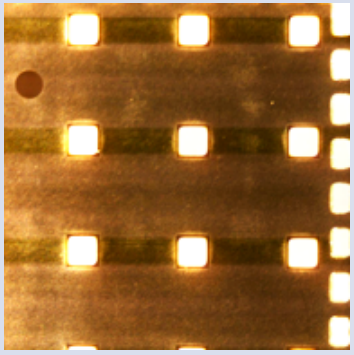
BGA (>200um metal balls)



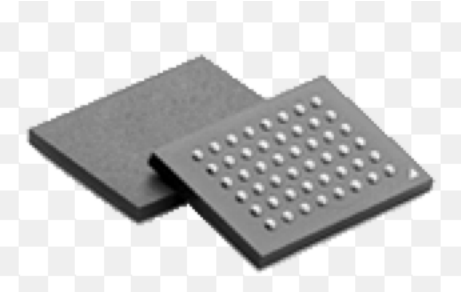
Bottom must be protected

Small Devices for Thermal Processing

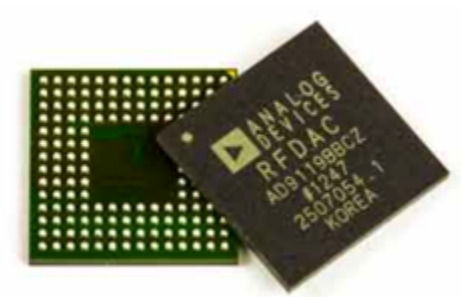
Appearance of Bottom

Name	#1	#2	#3
Dimension	0.95cm x 0.95cm	1.65cm x 1.15cm	0.95cm x 0.95cm
Overview			
Microscopic Picture			

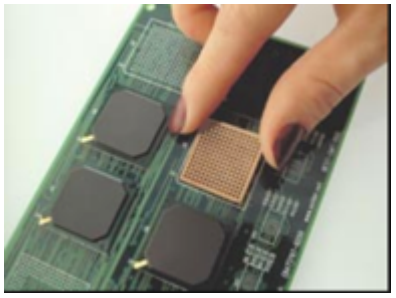
BGA Pkg Description



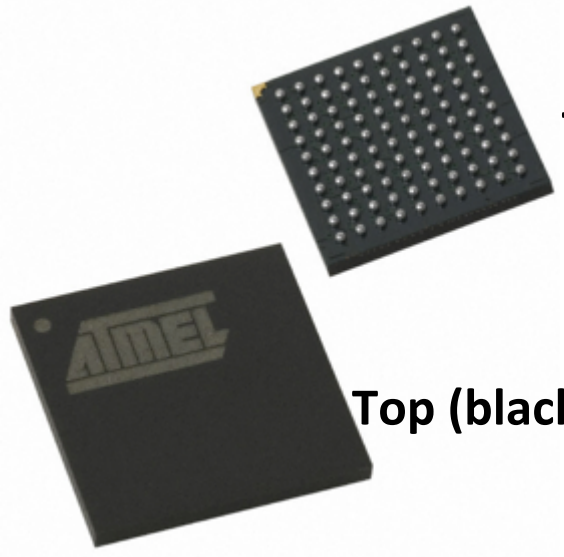
Many packages exist



Bottom (balls) & top

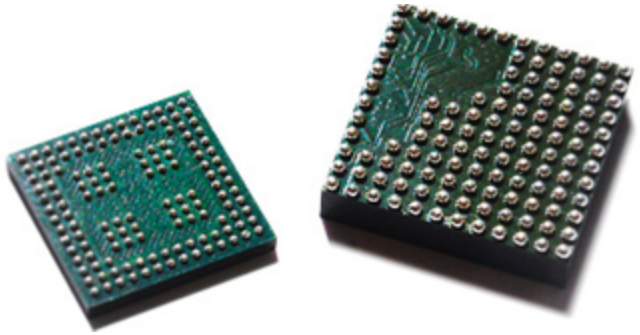


Size 25 X 25mm (above)
Can by much smaller



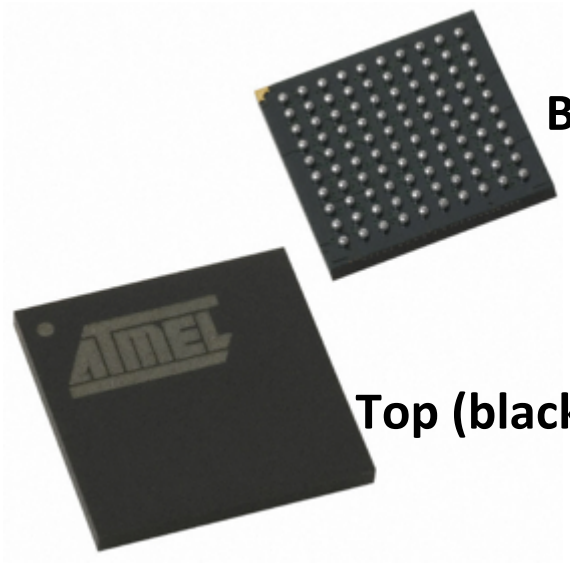
Bottom (balls)
Topography <300um

Top (black epoxy)



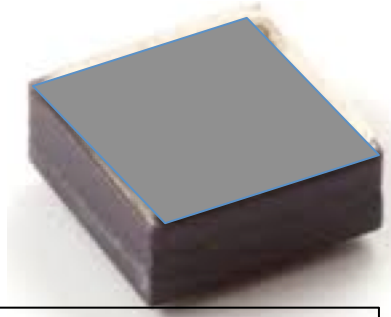
Bottom must be protected

EMI Shielding

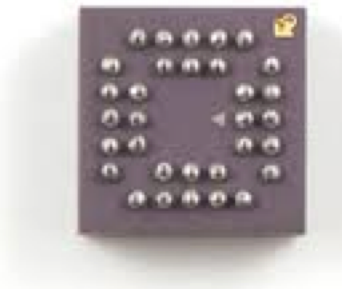


Bottom (balls)

Top (black epoxy)

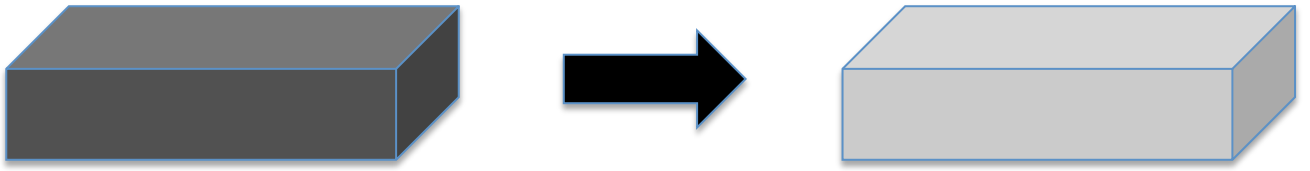


Top (and sides) must be coated with EMI shielding metal



Bottom must be protected from EMI coating

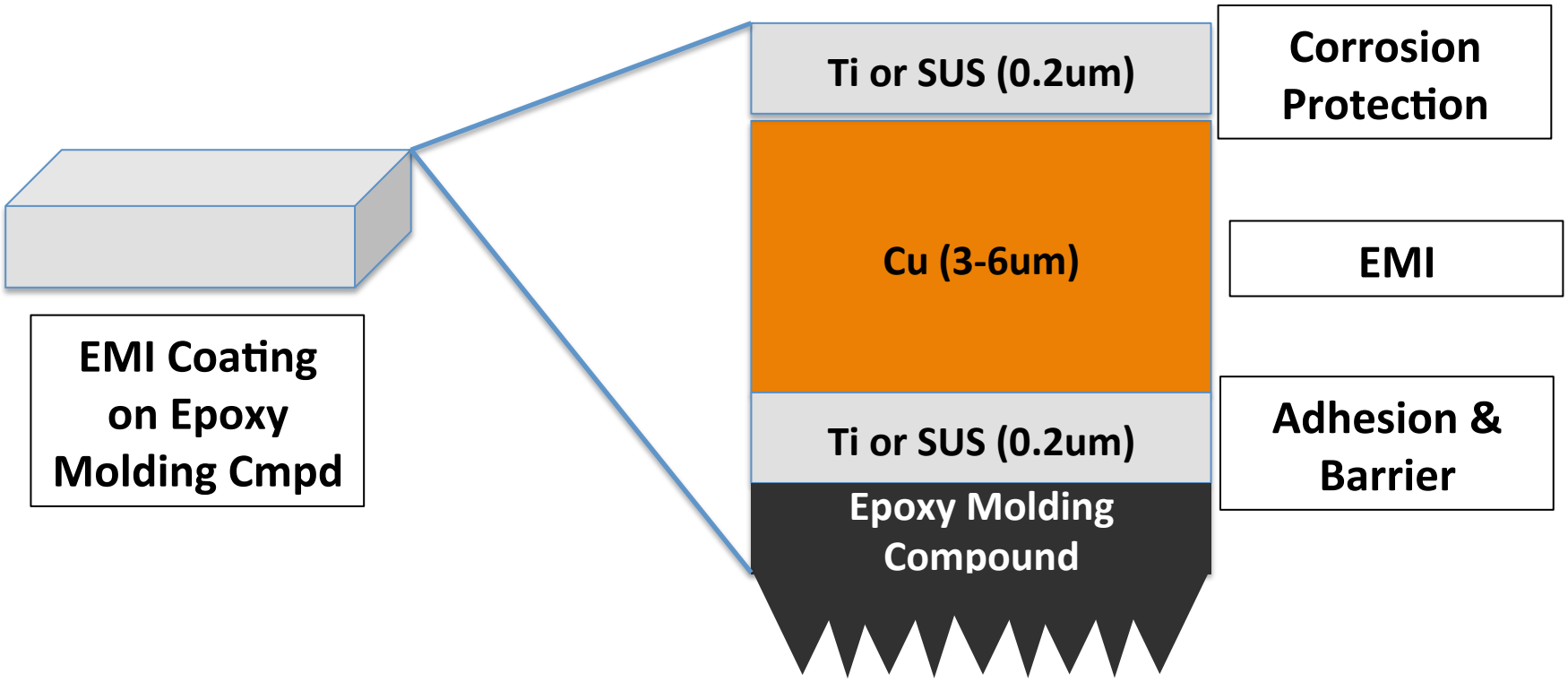
EMI Shielding



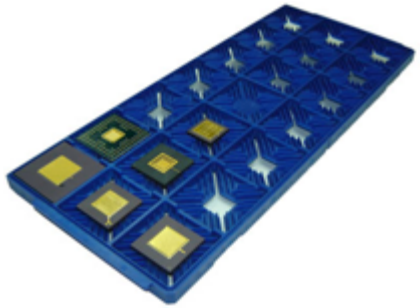
Top is an epoxy molding compound

EMI Shielding
Metal coatings
3-6um Cu
~0.2um "sandwich" – top & bottom of Cu (Ti or SUS)

EMI Shielding



Current Process Flow



Pkgs start & finish in JEDEC trays

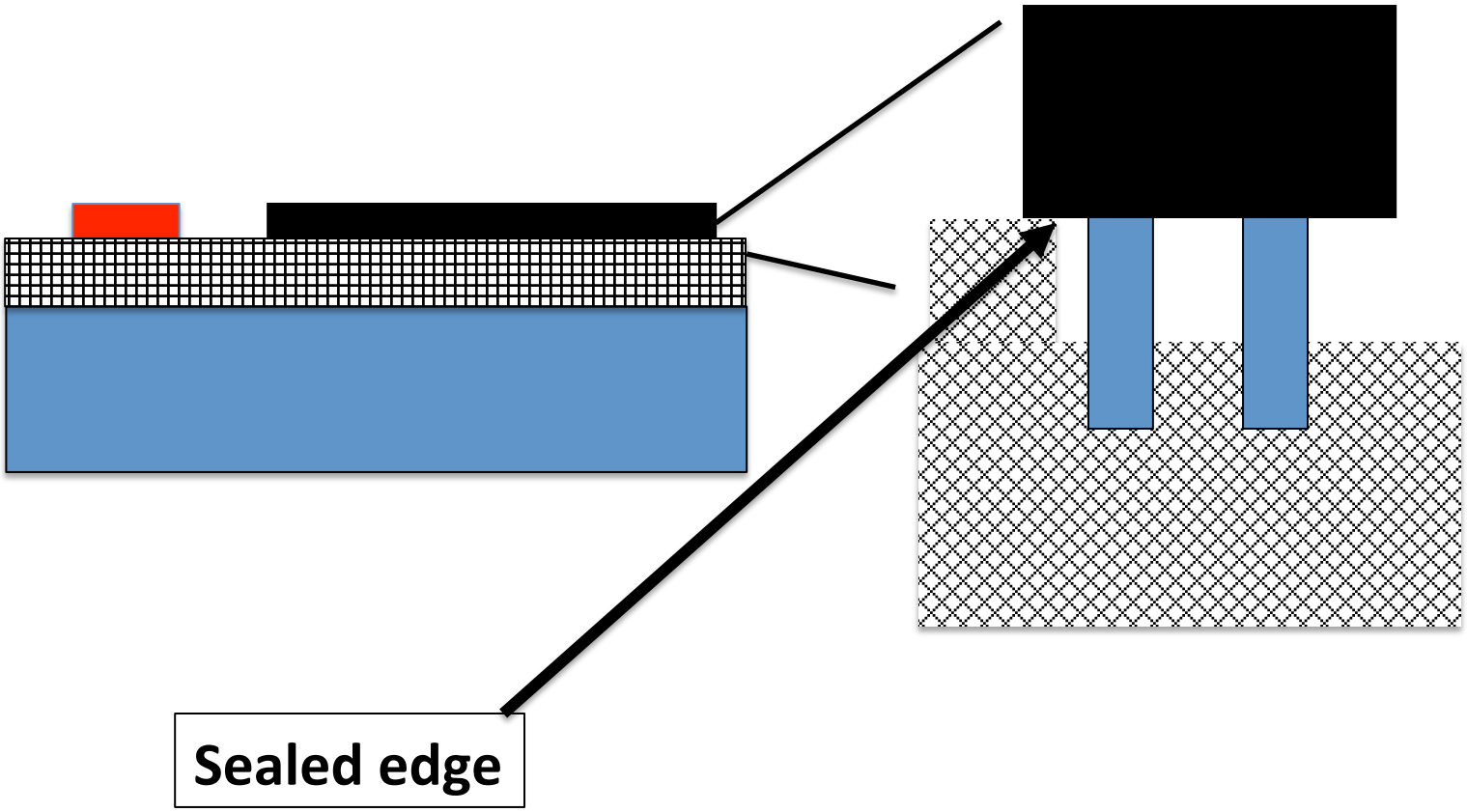
P&P Tool

Pkg Affixing & Removal

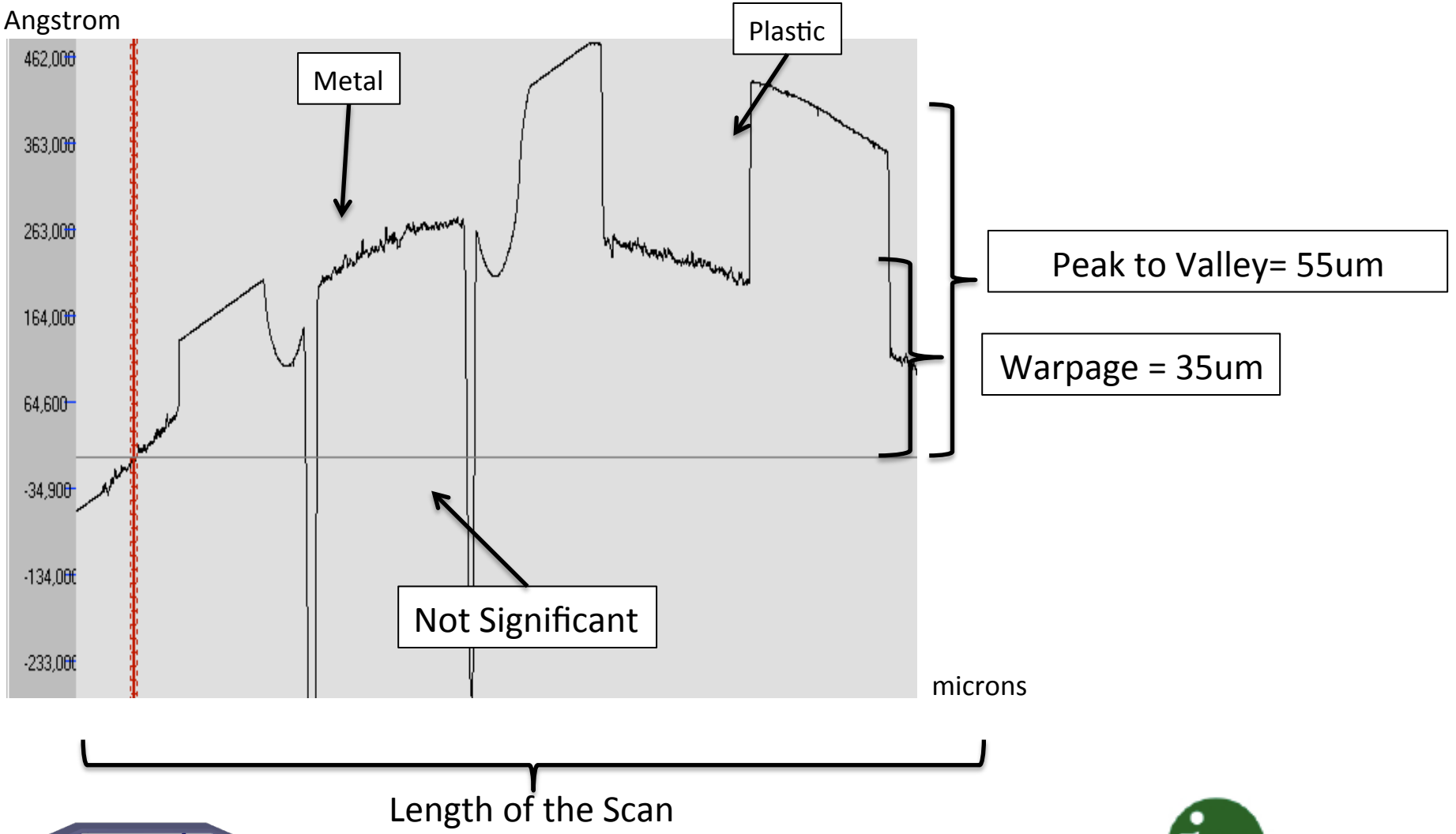
Adhesive Process

EMI Shielding Tool (Vacuum PVD)

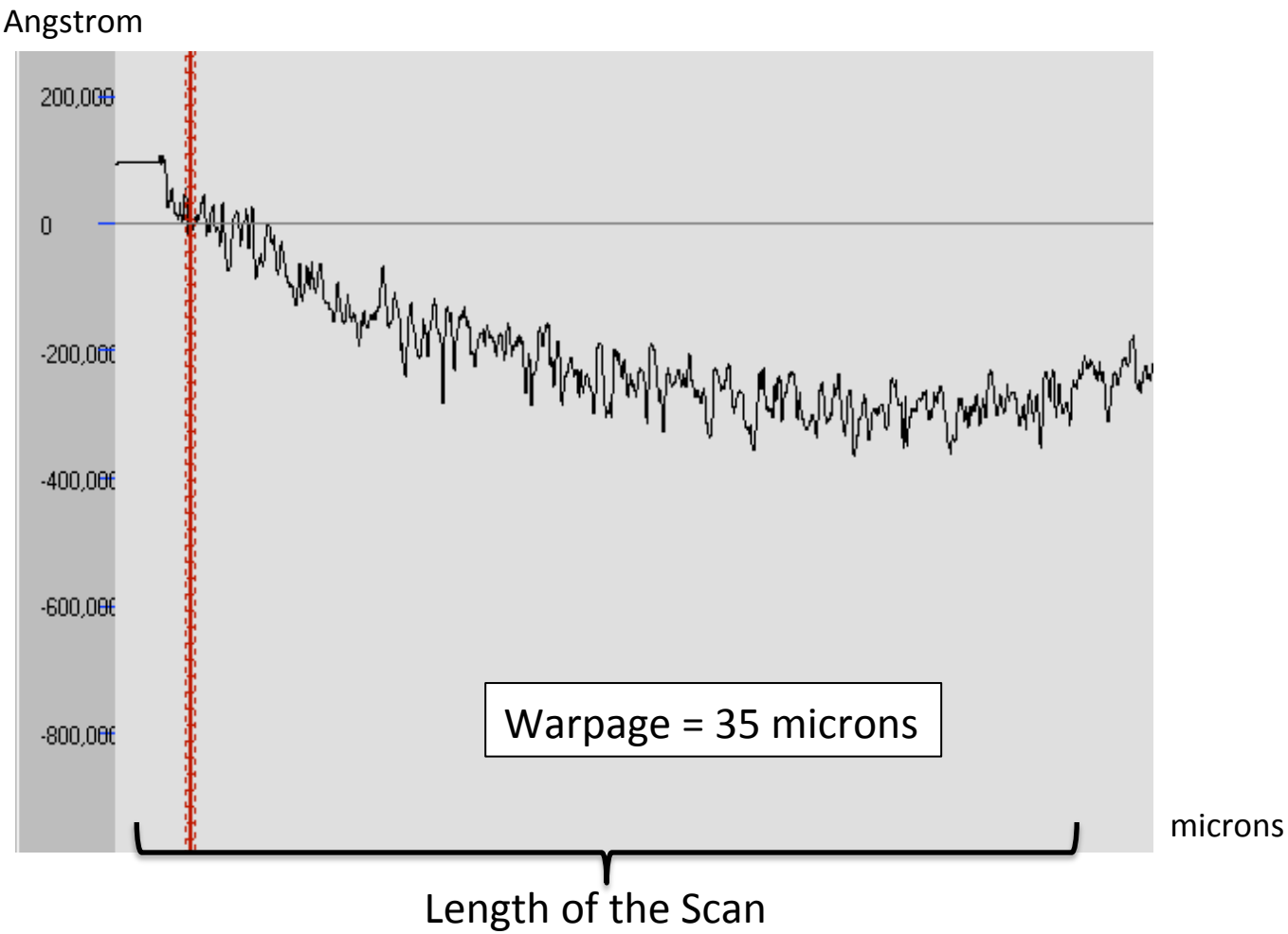
Component Bonding



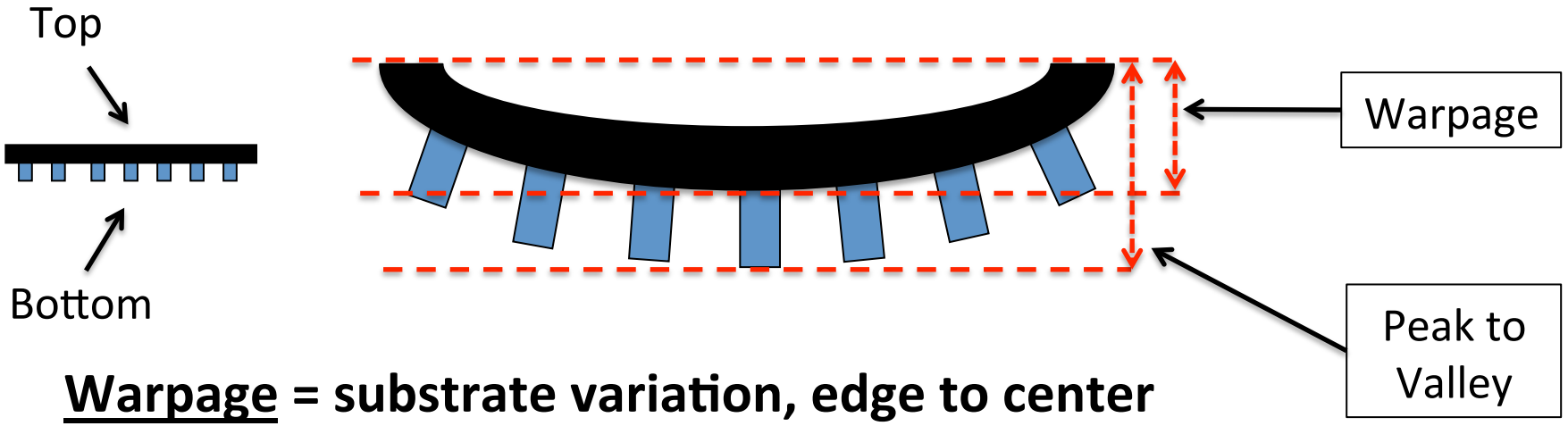
Surface Scan (Bottom of Substrate #1)



Surface Scan (Top of Substrate #1)



Substrate Description



<u>Warpage</u> = substrate variation, edge to center (no topography)

<u>Peak to valley</u> = min to max (with topography)

Ability to Bond & Seal w/Topography

Use of various DaeCoat products

Substrate	Peak to Valley (µm)	Warpage (µm)	Adhesive thickness <60µm	Adhesive thickness >60µm
#1	55	35	B	B
#2	14	<5	A	A
#3	26	23	B	B

A= Bond + Edge Seal (Ideal Process)
B= Bond

Summary

- Temporary bonding applied to wafers, displays, and devices – substrate support
- Must characterize substrate
- Choose adhesive and match to process needs
- Results suggest adhesive and carriers are demonstrated for substrates 4-10um, flexible, crystalline, using chemical and mechanical debond

Contact for More Information

- DAETEC provides development, consulting, and technical training/support to solve manufacturing problems and introduce new options of doing business.
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