Temporary Bonding of Wafers, Displays, and Components

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Daetec, LLC

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Contents

1. Adhesives & Substrates
2. Wafers
3. Displays
4. Devices
Electronics Everywhere

- Auto & Medical - diagnostics
- Aircraft - entertainment
- Communication
- IOT - surveillance & traffic
Thin Substrate Market Drivers

• Electronics trending thinner
• Smart phones, tablets, etc.
• Diced chips are stacked
• Stacked chips used in all functional devices
• Extremely fragile
• Requires a temporary support
1. Adhesives & Substrates

- Matched to substrate needs
- Surface energy (lower vs substrate)
- Thermal & chemical resistant
- Low outgas (high Tg or barrier)
- Inert & easy to clean
World of Temporary Bonding

<table>
<thead>
<tr>
<th>Work Unit</th>
<th>Market</th>
<th>DaeCoat™</th>
<th>Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Organic Film</td>
<td>OLED, flexible displays</td>
<td>350</td>
<td>Cure on carrier, bond w/pressure</td>
</tr>
<tr>
<td>Organic Film (cast)</td>
<td>OLED, flexible displays</td>
<td>310</td>
<td>Cure on carrier, cast &amp; cure liquid</td>
</tr>
<tr>
<td>Thin glass</td>
<td>TFT LCD</td>
<td>350</td>
<td>Cure on carrier, bond w/pressure</td>
</tr>
<tr>
<td>Foil</td>
<td>OLED, flexible displays</td>
<td>350</td>
<td>Cure on carrier, bond w/pressure</td>
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<tr>
<td>Wafer</td>
<td>3DIC</td>
<td>350, 615, 620</td>
<td>Planarize wafer w/550, cure on carrier, bond w/pressure</td>
</tr>
<tr>
<td>Die (chip)</td>
<td></td>
<td>350</td>
<td>Cure on carrier, bond w/pressure</td>
</tr>
</tbody>
</table>
Substrate Types

- **Rigid**: silicon, quartz, glass, sapphire
- **Flexible**: PI, PEN, Arylite, PPS, PET, epoxy
- **Ideal characteristics**: CTE match, low TTV
- **Other qualities**: transparency, tensile, barrier
- **Dimensions**: application specific
Engineering Polymers

PBI Tg = 427 °C

PI Tg = 370 °C
Typical PI Transparency Thermal Trend

Inert N2 atmosphere
Silicone Thermoset (catalytic)

Resin monomer (MW & shape) → Free-Radical

Activator monomer (MW & shape) + Silicone Polymer
Effects of Post-Bake on Outgassing from Vinyl Silicone

Thermal Stability % vs. Temperature (C) for different conditions:
- No PB
- PB 250C
- PB 300C
- PB 350C

Testing in Air
Silicone 400C Thermal Resistance

Silica Effect on Thermal Stability of Silicone Silanol

Thermal Stability (%) vs. Silica Nanoparticle (%)

- 0% Silica: 97.0%
- 0.1% Silica: 99.6%
- 1% Silica: 99.7%
- 5% Silica: 99.4%
- 10% Silica: 99.0%
- 20% Silica: 97.2%

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Adhesive in Several Forms

Liquid

Gel

Film
Peripheral Bond

• The adhesive may be applied on the edges of the carrier – known as peripheral bond
• Thin substrate is bonded onto carrier
• Adhesive undergoes heat cure
Negative PR Stripping Bath Life WPG vs. Wafer Size

Solvent  Aqueous

Bath Life (WPG)

Wafer Diameter (inches)
2. Wafers

- Wafers thinned to <100um
- Carriers are required
- Debonding generates problems, can be a bottleneck, high cost, and source of yield loss
Creating a Process

• Device Wafer: planarized, edge trim (thickness)
• Carrier: CTE closely matched, TTV <2um
• Adhesive: thermal & chemical resistant, thin & uniform, if thick (high modulus)
• Bond: low temp (CTE)
• Debond: passive & cleans complete
Planarization Coating

Wafer with Topography (planarize >100um)

Planarization Coating

Planarized Surface

DaeCoat™ 515 – DIW washable
Carriers

- Silicon
- Glass
- Sapphire
- Tape

Porous Carriers
Perforated Glass, 50 μm

Divots from glass pores

Surface Scan shows the divots from glass pores
Porous Carrier

Benefits

- Thermal & chemical resistant
- Simple bond, high adhesion
- Accepts many adhesive types
- Passive debond (chemical diffusion)
- Device wafer on film frame
- Recycle >10X
Porous Metal Carrier Media

Req. 1410371: Roughness on sintered material

- Smooth (lowest Ra) in the product line
- Mid-range smooth product
- Ti is only non-ferrous product acceptable by fabs
Ti Porous Metal (Microscopic)
Surface Scan of Porous Ti

Ti has stray wires reaching <80μm

~80μm
Porous Metal Carrier

Polishing to TTV
Surface Treatment

Without Exclusion Layer

With Exclusion Layer

Wetting

No wetting
Wafer Grinding & Testing

- Use a local grind/polish firm (Arizona, USA)
- Equipment is consistent with that used in fabs
- Scientists have a high degree of experience
## Commercial Technologies

<table>
<thead>
<tr>
<th>Bond type</th>
<th>BSI (Zonebond)</th>
<th>3M</th>
<th>TMAT</th>
<th>Dupont</th>
<th>Dow Corning</th>
<th>DOW</th>
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<tbody>
<tr>
<td>Thermoplastic</td>
<td>Thermoset</td>
<td>Thermoset</td>
<td>Thermoset</td>
<td>Thermoplastic</td>
<td>Thermoset</td>
<td>Thermoplastic</td>
</tr>
<tr>
<td>Slide + CRT /Peel</td>
<td>Laser, Peel</td>
<td>Peel</td>
<td>Laser + CRT</td>
<td>Peel</td>
<td>Peel</td>
<td>Peel</td>
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<tr>
<td>Thermoplastic</td>
<td>Thermoset</td>
<td>Thermoset</td>
<td>Thermoset</td>
<td>Thermoplastic</td>
<td>Thermoset</td>
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<td>Laser tool, Peel tool</td>
<td>Peel tool</td>
<td>Peel tool</td>
<td>Laser tool, Peel tool</td>
<td>Peel tool</td>
<td>Peel tool</td>
<td>Peel tool</td>
</tr>
<tr>
<td>Thermoplastic</td>
<td>Thermoset</td>
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<td>Thermoset</td>
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<td>Peel tool</td>
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</tr>
<tr>
<td>Cleans, tape isolation</td>
<td>Cleans, Tape isolation</td>
<td>Cleans, Tape isolation</td>
<td>Cleans, Tape isolation</td>
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<tr>
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<td>Cleans, Tape isolation</td>
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<td></td>
</tr>
<tr>
<td>≤250°C</td>
<td>≤250°C</td>
<td>≤300°C</td>
<td>≤450°C</td>
<td>≤300°C</td>
<td>&gt;300°C</td>
<td></td>
</tr>
<tr>
<td>Cleans</td>
<td>Transparent carriers</td>
<td>None</td>
<td>Transparent carriers</td>
<td>Lengthy curing cycle</td>
<td>Cleans</td>
<td>None</td>
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<tr>
<td>RT Debond</td>
<td>RT Debond</td>
<td>RT Debond</td>
<td>High temp processing, RT debond</td>
<td>RT Debond</td>
<td>High temp processing, RT debond</td>
<td></td>
</tr>
</tbody>
</table>
Process Flow – Porous Carrier

**Silicon Substrate**

- **Spin Coat Adhesive**
  - Apply Adhesive to silicon device

- **Cure Adhesive**
  - Prepare for Dry-bond

- **Dry-Bond**
  - 25-30C, 5min in Bonder
  - (Pressure ~15psi)

**Subsequent Steps**

- Thin Debond
3. Displays

Cured DaeCoat 310 Adhesive

Adhesive on substrate (Si or glass)

Cured PI or similar cured on substrate w/adhesive

PL or similar cured on substrate w/adhesive

Customer Device Processing

- LTPS
- Lithography
- Etch
- Bake

Film Removal

- Roll peel
- Center region specific

- Lift-peel
- Center region specific
Discussion

Peel force applied by and measured by meter

Tensile strength as exhibited by polymer

Adhesive strength as exhibited by adhesive layer

Model of thin substrate peeling with adhesive layer, minimizing bubble formation
Bubble Model

Bubble forms when force of irregularity > adhesive

Force exhibited by gas or other irregularities

Adhesive strength as exhibited by adhesive layer
Adhesive: DaeCoat™ 310

**DaeCoat 310 Mix**

Mix A,B and C Filter (0.2micron)

**Slit Coating:**
1. Adjust Gap height (<1 µm)
2. Apply

**Spin Coating:**
1. Dispense
2. 500rpm (60sec)

**Curing**
1. 150°C (5min)
2. 250°C (15min)
PI or Similar Coating
Daetec’s Polyimide: DaeCoat™ 210

**Slit Coating:**
1. Adjust Gap height (10-40µm)
2. Apply

**Spin Coating:**
1. Dispense
2. 1000-2000rpm (60sec)

**Curing**
1. 150°C (5min)
2. 250°C (15min)
3. 350°C (10min)

Cured DaeCoat™ 310

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Peel Force of Liquid Cast Materials
Thickness: ~20microns

- Film pulled at 90° Configuration
- Peel Force can be tuned to meet customer’s processes

<table>
<thead>
<tr>
<th>Material</th>
<th>Peel Force (gF/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polyimide</td>
<td>5</td>
</tr>
<tr>
<td>Polyamide-imide</td>
<td>40</td>
</tr>
<tr>
<td>DaeCoat 200</td>
<td>1</td>
</tr>
<tr>
<td>Fluorinated Polyester</td>
<td>40</td>
</tr>
</tbody>
</table>
Adhesive Force of DaeCoat™ 310
With Daetec’s PI: DaeCoat™ 210

Peel Force (gF/cm)

<table>
<thead>
<tr>
<th>Ratio</th>
<th>Peel Force</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:1 A:B</td>
<td>100</td>
</tr>
<tr>
<td>8:2 A:B</td>
<td>90</td>
</tr>
<tr>
<td>7:3 A:B</td>
<td>80</td>
</tr>
<tr>
<td>6:4 A:B</td>
<td>70</td>
</tr>
<tr>
<td>5:5 A:B</td>
<td>60</td>
</tr>
</tbody>
</table>

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High Volume Manufacturing

DaeCoat 310 – P1
DaeCoat 310 – P2

Drum = 200L

Mix & Dispense Tooling

Spin Coating

DaeCoat™ 310 components are stable for long shelf-life prior to mixing.
Glass on Glass Bonding

- To prevent fusion, carrier is treated
- Allows glass substrate to debond after high temp processing

Surface Treated Glass Carrier → Bond, Process (>300C) → Adhesive Removal → Debond OK
Controlled Adhesion: Edge Pull

Low Bond Force Weaker Adhesive

170um Glass Peel

Peel Force (gF) vs Time (sec)
4. Devices

*Thin Silicon Interposers (TSIs)*

- Substrate ~100um thickness
- Underlying bumps ~100um height

---

**Top side**

**Bottom side**

(contains solder bumps)
Application

1 Substrate w/Topography

2 Application Coverage

3 Cure to Planarize

4 Apply/Cure to Carrier

5 Apply to Substrate Bond to Carrier

6 Cure to Mount

Recyclable porous substrate
Post-Bonding Process

7 Customer Process

Bonded interposer
attach chips to
interposer
Reflow 250-300C

8 Debond & Cleans
Debond and Cleans
rinse, dry
Recycle carrier

9 Acquire Final Product

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Adhesive Planarization

No adhesive

~75% Bump height

Adhesive
Planarization and Thermal

- Voids -

Serious Damage

No Voids

No Damage

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Porous Carrier

Porosity higher for inside material (A). Outer coating (B) is lower porosity.

A = 0.5 – 0.8mm
B = 0.1 - 0.25mm
C = 0.5 – 1mm
Results – baseline TSI
Results – Bonded TSI

Variation <12um
Profilometry Measurement of Bow vs. Process Condition

- **Max**
- **Ave**

Measured Bow (um)

- Free Standing Interposers
- Affixed Interposers

<table>
<thead>
<tr>
<th>Process Condition</th>
<th>Type</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>H1</td>
<td>1, 2, F</td>
<td>Peripheral</td>
</tr>
<tr>
<td>H2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>NW</td>
<td>Porous Subst</td>
</tr>
<tr>
<td>2</td>
<td>NW</td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>NW</td>
<td></td>
</tr>
<tr>
<td>NW1</td>
<td>NW</td>
<td></td>
</tr>
<tr>
<td>NW2</td>
<td>NW</td>
<td></td>
</tr>
<tr>
<td>NW3</td>
<td>NW</td>
<td></td>
</tr>
</tbody>
</table>

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Bow Reduction of Affixed Interposer Die

Reduction as % of original condition

H1: 69.9%
H2: 87.8%
L: 73.8%
Results – DeBonding

1. Prior activity involved applying adhesive to interposer & silicon wafer, holding interposer in place.
2. Bond interposer to silicon wafer, observe flatness and other process details.
3. Debond from silicon in Daetec digesting fluid, observe time.
Devices (cont.)

- Desire to attach device, process, remove with no residue. Adhesive is thermal & chemical resistant, conforms to device substrate
- Various adhesives are available
- Device substrates can be irregular
- Bond/edge seal (A) desired, best w/thickness
- Adhesive may be applied by several methods
- Carrier recycle with cleaning
- Total cost must be considered
Component Bonding

Sealed edge
Small Devices for Thermal Processing

**Appearance of Bottom**

<table>
<thead>
<tr>
<th>Name</th>
<th>#1</th>
<th>#2</th>
<th>#3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>0.95cm x 0.95cm</td>
<td>1.65cm x 1.15cm</td>
<td>0.95cm x 0.95cm</td>
</tr>
<tr>
<td>Overview</td>
<td><img src="image1.png" alt="Image of #1" /></td>
<td><img src="image2.png" alt="Image of #2" /></td>
<td><img src="image3.png" alt="Image of #3" /></td>
</tr>
<tr>
<td>Microscopic Picture</td>
<td><img src="image1_micro.png" alt="Image of #1 Microscopic" /></td>
<td><img src="image2_micro.png" alt="Image of #2 Microscopic" /></td>
<td><img src="image3_micro.png" alt="Image of #3 Microscopic" /></td>
</tr>
</tbody>
</table>
Process Description

Parts Mounting

Coating cure

Thermal Processing

Treatment
Adhesive is applied as a film to carrier on Thick Glass, Open-Faced
Substrate Description

**Warpage** = substrate variation, edge to center
(no topography)

**Peak to valley** = min to max (with topography)
Surface Scan (Bottom of Substrate #1)

Metal

Plastic

Peak to Valley = 55um
Warpage = 35um

Not Significant

Length of the Scan

Angstrom

microns

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Surface Scan (Top of Substrate #1)

Warpage = 35 microns

Length of the Scan

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## Ability to Bond & Seal w/Topography

Use of various DaeCoat products

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Peak to Valley (μm)</th>
<th>Warpage (μm)</th>
<th>Adhesive thickness &lt;60μm</th>
<th>Adhesive thickness &gt;60μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>55</td>
<td>35</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>#2</td>
<td>14</td>
<td>&lt;5</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>#3</td>
<td>26</td>
<td>23</td>
<td>B</td>
<td>B</td>
</tr>
</tbody>
</table>

A= Bond + Edge Seal (Ideal Process)
B= Bond
Adhesive Film - Options

1. Use as B-stage film, thickness can vary
2. Slit-coating to substrates, SB cure, process as desired
Film w/Release Layers

- Aqueous-based adhesive
- Thickness = 20mil ~500um ~0.5mm
- No backing
- Sandwiched between PET release layers
- Remove 1\textsuperscript{st} PET liner, apply to substrate
- Use a rubber roller, apply exposed adhesive to substrate, increase pressure onto PET facing up, remove 2\textsuperscript{nd} PET liner, proceed with bonding
Slit Coating
## Cost Considerations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Film w/release liners</th>
<th>Spin Coating</th>
<th>Slit Coating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coating solids (%)</td>
<td>80-100</td>
<td>&lt;100</td>
<td>100</td>
</tr>
<tr>
<td>Cost ($/cm2)*</td>
<td>&lt;0.05</td>
<td>&lt;0.05</td>
<td>&lt;0.02</td>
</tr>
<tr>
<td>Convenience</td>
<td>High</td>
<td>Med</td>
<td>Med</td>
</tr>
<tr>
<td>Tool Required</td>
<td>-none-</td>
<td>coater</td>
<td>coater</td>
</tr>
</tbody>
</table>

*assume best case conditions with max solids for coating capability
UV Cure Film/Coating

Parts Mounting

UV Curing (<1min) + Thermal Outgas (<200°C 5min)

Customer Process

Thermal Process

Storage/Other Process

Debond Wash
Debond/Rinsing

Low-cost tape film

DIW safe
Holds parts

Film Frame Attach

DIW Wash

Debond

Pick & Place

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Summary

- Temporary bonding technologies are being used for wafers, displays, and devices
- Key practices include variations around peel practices
- Cross-pollination continues to drive more creative development in different markets
- Improved yield, cost control, and simplicity are drivers
Contact for More Information

• DAETEC provides development, consulting, and technical training/support to solve manufacturing problems and introduce new options of doing business.

• Diversified Applications Engineering Technologies (DAETEC)
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